FH8550M

HD Analog CMOS ISP Chip

User Datasheet

Rev：1.4

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Introduction

This document is a brief introduction of FH8550M chip.

Revision History

Date	Rev	Owner	Description
2017/08/25	V1.1	Hu	Initial
2020-03-12	V1.2	Ryan	Update address
2020-04-21	V1.3	Ryan	Update package overall height and lead width
2023-11-9	V1.4	Ryan	Change pin41 name in Pin Map to be consistent with Pin Arrange

CONTENTS

1. Outline

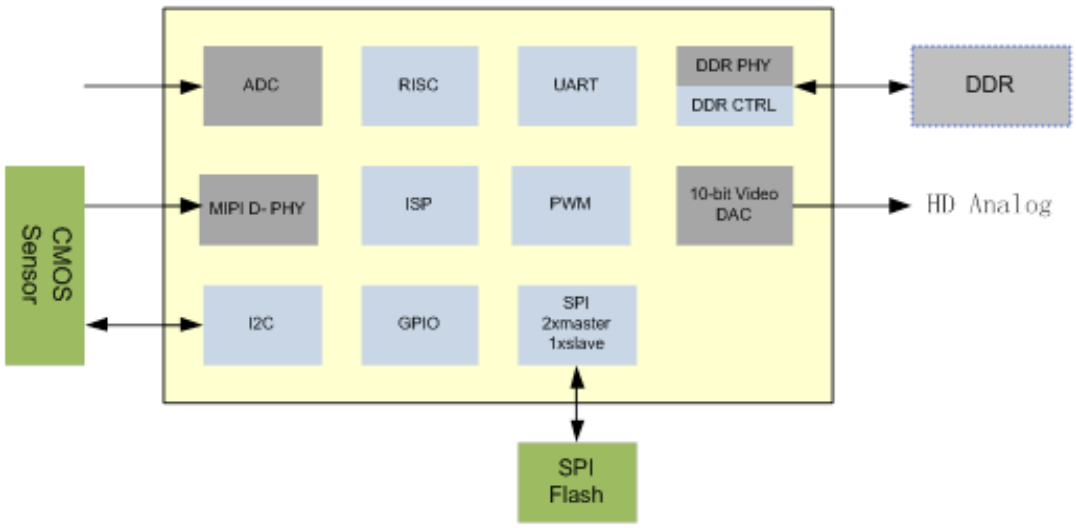
FH8550M is an ISP for CIS (CMOS Image Sensor) and targeted on professional surveillance CCTV camera. FH8550M supports 1M/2M Pixel CIS with MIPI input. It supports high performance image processing technology including 3D de-noise, AF, WDR, and so on. Its video outputs support standard CVBS/960H/1280H and 720P60/50/30/25, 1080P30/25.

1.1 Feature

Table 1 Feature

FEATURE	DESCRIPTION		
Support 3D de-noise	**Input**	Support RGB Bayer	
Support WDR		Support 2M/1.3M/1.0M	
Support AE/AWB/AF		Support MIPI	
Support sensitive areas shielded		Clock effective edge & Frame, Line effective edge is configurable	
Support 720p/1080p HD-Analog output	**Output**	Standard CVBS/960H/1280H 720p@25fps/30fps/50fps/60fps HD Analog 1080p@25fps/30fps HD Analog	
Support RS485 Up the Coax function			
TOSD	**Memory**	SPI flash external	
GOSD	**Interface**	I2C×1（Master）（Multiplexing）	
DDR Internal		UART×2（Multiplexing）	
Support LSC		GPIO×28（Multiplexing）	
Adaptive 2D de-noise		SPI×3（Master x2,Slave x1）（Multiplexing）	
Y/C de-noise		SADC×3（Multiplexing）	
Support LTM statistics		PWM×8（Multiplexing）	
Support move detect		I2S×1（Multiplexing）	
High performance CFA interpolation	**Power**	I/O	1.8v or 3.3v
Support Sensor FPN		Core	1.2v
Support auto bad points detect and delete		DDR	1.8v
Support auto black eliminated		Analog	3.3v
Adaptive Sharpness	**Package**	QFN68（8mm×8mm. Pitch=0.4mm）	

2. Block Diagram



3. Feature

3.1 CIS Input

- Support up to 2.0M CMOS sensor
- MIPI Interface
- Clock effective edge & Frame, Line effective edge is configurable

3.2 ISP

- Support LSC
- Reduce fixed pattern noise
- Support 3D de-noise
- Adaptive 2D de-noise, support Y/C de-noise
- Support high performance WDR
- Support image information statistics
- Support AE statistics

- Support AWB statistics
- Support AF statistics
- Support LTM statistics
- Support AE/AWB/AF
- Support 256 areas move detect
- Support auto exposure
- High performance CFA interpolation
- Support color correction
- Support Gamma correction，Gamma table is configurable
- Support sensitive areas shielded
- Support OSD
- Video Enhancement: Brightness, sharpness , contrast and saturation adjustment

3.3 Video Output

- Support HD-Analog Output
- Support HD-Analog Output：1920x1080@25fps/30fps, 1280x720@50fps/60fps
- Support CVBS Output：Standard CVBS，960H，1280H
- Support RS485 Up the Coax function

3.4 External Interfaces

- I2C
- 3xSPI, SPI0(master), SPI1(master), SPI2(slave)
- 28 bit GPIO
- 2xUART, UART0 for debug, UART1 for printout
- 3xSAR-ADC
- 8xPWM
- I2S

3.5 Others

- System Clock 27MHz
- Typical Power Dissipation ≤ 590mW
- Operating Temperature -20℃~70℃
- Package QFN68（8mmx8mm，pitch=0.4mm）

4. Pin Descriptions

4.1 Pin Descriptions

4.1.1 Pin Map

		GPIO_30/UART1_TX	VDDIO_33	VDD	GPIO_23/RS485	PLL_VSSA	PLL_VDDA	SADC_CH2	SADC_CH1	SADC_CH0	SADC_DAC_VSSA	SADC_VDDA	DAC_REXT	DAC_COMP	DAC_VDDA	DAC_CVBS	MIPI_D3_N	MIPI_D3_P		
		68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52		
GPIO_31/UART1_RX	1																		51	MIPI_D2_N
GPIO_0/UART0_TX	2																		50	MIPI_D2_P
GPIO_1/UART0_RX	3																		49	MIPI_VSSA
GPIO_4/SPI0_CS/SPI2_CS	4																		48	MIPI_CLK_N
GPIO_5/SPI0_CLK/SPI2_CLK	5																		47	MIPI_CLK_P
GPIO_6/SPI0_TXD/SPI2_TXD	6																		46	MIPI_RBIAS
GPIO_7/SPI0_RXD/SPI2_RXD	7																		45	MIPI_D1_P
RESETN	8																		44	MIPI_D1_N
DDRIO_18	9																		43	MIPI_D0_P
DDRIO_18	10																		42	MIPI_D0_N
VDD	11																		41	MIPI_VDDA
GPIO_11/I2S_CLK	12																		40	TEST
GPIO_14/I2S_WS	13																		39	VDD
GPIO_15/I2S_TXD	14																		38	DDRIO_18
GPIO_16/I2S_RXD	15																		37	DDRIO_18
CLK_OUT	16																		36	GPIO_25
CLK_IN	17																		35	VDDIO_18
		18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34		
		VDDIO_33	GPIO_8(IRCUT_OFF)	GPIO_9(IRCUT_ON)	GPIO_2/PWM0	GPIO_3/PWM1	GPIO_17/PWM2/I2S_MCLK	GPIO_18/PWM3/SPI1_CS0	GPIO_19/PWM4/SPI1_CS1	GPIO_20/PWM5/SPI1_CLK	GPIO_21/PWM6/SPI1_TXD	GPIO_22/PWM7/SPI1_RXD	VDD	GPIO_10(CIS_RST)	CIS_CLK	CIS_SCL/GPIO_12	CIS_SDA/GPIO_13	GPIO_24		

Pin diagram（Top View）

4.1.2 Pin Arrangement

Pin Position	Pin Name	Type	Description
System Signals			
17	CLK_IN	I	27MHz System Clock Input
16	CLK_OUT	O	27MHz System Clock Output
8	RESET	I	System Reset Input, （BANK2 IO POWER DOMAIN） 0:System Reset, 1:Normal Work
40	TEST	I	TEST Mode Select:（Internal Low，BANK1 IO POWER DOMAIN） 0:Normal 1:Test Mode
MIPI Interface			
31	CIS_CLK	O	CIS_CLK（BANK1 IO POWER DOMAIN）
30	CIS_RESET	O	Sensor Reset, Active Low（BANK1 IO POWER DOMAIN）
48	MIPI_CLK_N	O	MIPI_CLK_N（BANK1 IO POWER DOMAIN）
47	MIPI_CLK_P	O	MIPI_CLK_P（BANK1 IO POWER DOMAIN）
42	MIPI_D0_N	O	MIPI_D0_N（BANK1 IO POWER DOMAIN）
43	MIPI_D0_P	O	MIPI_D0_P（BANK1 IO POWER DOMAIN）
44	MIPI_D1_N	O	MIPI_D1_N（BANK1 IO POWER DOMAIN）
45	MIPI_D1_P	O	MIPI_D1_P（BANK1 IO POWER DOMAIN）
51	MIPI_D2_N	O	MIPI_D2_N（BANK1 IO POWER DOMAIN）
50	MIPI_D2_P	O	MIPI_D2_P（BANK1 IO POWER DOMAIN）
53	MIPI_D3_N	O	MIPI_D3_N（BANK1 IO POWER DOMAIN）
52	MIPI_D3_P	O	MIPI_D3_P（BANK1 IO POWER DOMAIN）
46	MIPI_RBIAS	O	MIPI_RBIAS
41	MIPI_VDDA	P	MIPI Power Supply Internal (1.2V)
49	MIPI_VSSA	G	MIPI Ground
GPIO			
2	GPIO_0	I、O	GPIO（BANK2 IO POWER DOMAIN）
3	GPIO_1	I、O	GPIO（BANK2 IO POWER DOMAIN）
21	GPIO_2	I、O	GPIO（BANK2 IO POWER DOMAIN）
22	GPIO_3	I、O	GPIO（BANK2 IO POWER DOMAIN）
4	GPIO_4	I、O	GPIO（BANK2 IO POWER DOMAIN）
5	GPIO_5	I、O	GPIO（BANK2 IO POWER DOMAIN）
6	GPIO_6	I、O	GPIO（BANK2 IO POWER DOMAIN）
7	GPIO_7	I、O	GPIO（BANK2 IO POWER DOMAIN）
19	GPIO_8	I、O	GPIO（BANK2 IO POWER DOMAIN）
20	GPIO_9	I、O	GPIO（BANK2 IO POWER DOMAIN）
12	GPIO_11	I、O	GPIO（BANK2 IO POWER DOMAIN）

13	GPIO_14	I、O	GPIO（BANK2 IO POWER DOMAIN）
14	GPIO_15	I、O	GPIO（BANK2 IO POWER DOMAIN）
15	GPIO_16	I、O	GPIO（BANK2 IO POWER DOMAIN）
23	GPIO_17	I、O	GPIO（BANK2 IO POWER DOMAIN）
24	GPIO_18	I、O	GPIO（BANK2 IO POWER DOMAIN）
25	GPIO_19	I、O	GPIO（BANK2 IO POWER DOMAIN）
26	GPIO_20	I、O	GPIO（BANK2 IO POWER DOMAIN）
27	GPIO_21	I、O	GPIO（BANK2 IO POWER DOMAIN）
28	GPIO_22	I、O	GPIO（BANK2 IO POWER DOMAIN）
65	GPIO_23	I、O	GPIO（BANK2 IO POWER DOMAIN）
34	GPIO_24	I、O	GPIO（BANK1 IO POWER DOMAIN）
36	GPIO_25	I、O	GPIO（BANK1 IO POWER DOMAIN）
68	GPIO_30	I、O	GPIO（BANK2 IO POWER DOMAIN）
1	GPIO_31	I、O	GPIO（BANK2 IO POWER DOMAIN）
I2C			
32	CIS_SCL	O	I2C CLK（BANK1 IO POWER DOMAIN）
33	CIS_SDA	I、O	I2C DATA（BANK1 IO POWER DOMAIN）
DAC			
56	DAC_COMP	I、A	Video DAC Compensation Input
54	DAC_CVBS	O、A	Video DAC Video DAC Video Output
57	DAC_REXT	I、A	Video DAC Configuration Resistance
55	DAC_VDDA	P、A	Video DAC Power Supply (3.3V, connect with SDAC_VDDA internal)
SADC			
60	SADC_CH0	I、A	SADC CH0 Input
61	SADC_CH1	I、A	SADC CH1 Input
62	SADC_CH2	I、A	SADC CH2 Input
58	SADC_VDDA	P、A	SADC Power Supply (3.3V， connect with DAC_VDDA internal)
59	SADC_VSSA	P、A	SADC Ground
PLL			
63	PLL_VDDA	P	PLL Power Supply Internal (1.2V)
64	PLL_VSSA	G	PLL Ground
Power / Ground			
9、10、37、38	DDRIO_18	P	DDR Power Supply（1.8V）
11、29、66、39	VDDK	P	Core Power Supply（1.2V）
35	VDDIO_BANK1	P	BANK1 IO Power Supply（1.8V or 3.3V）
18、67	VDDIO_BANK2	P	BANK2 IO Power Supply（3.3V）

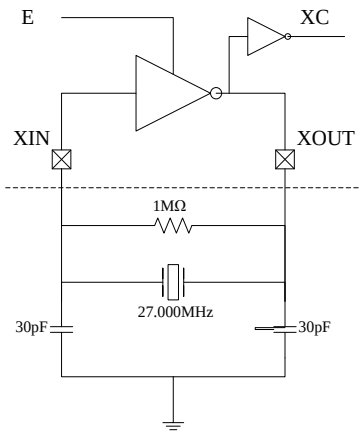
4.1.3 GPIO Descriptions

GPIO	Name	Direction	PU/PD	Description
0	FPN	I	U	1:Normal; 0:FPN
	UART0_TX	O		UART Interface
1	UART0_RX	I	U	
2	BOOT_SEL0	I	D	BOOT_SEL0 Default (with pull down resistor internal) ｛BOOT_SEL1, BOOT_SEL0｝=00，SPI Flash normal work ｛BOOT_SEL1, BOOT_SEL0｝=01，SPI slave mode ｛BOOT_SEL1, BOOT_SEL0｝=1x，Xmodem update mode
	PWM0	O		Multiplexing：PWM0
3	BOOT_SEL1	I	D	BOOT_SEL1 Default (with pull down resistor internal)
	PWM1	O		Multiplexing：PWM1
4	GPIO_4	O	U	GPIO
	SPI0_CS	O		SPI0_CS
	SPI2_CS	O		SPI2_CS
5	SPI0_CLK	O	D	SPI0_CLK
	SPI2_CLK	O		SPI2_CLK
6	SPI0_TXD	O	D	SPI0_TXD
	SPI2_TXD	O		SPI2_TXD
7	SPI0_RXD	I	D	SPI0_RXD
	SPI0_RXD	I		SPI2_RXD
8	IRCUT_OFF	O	U	IRCUT_OFF
9	IRCUT_ON	O	U	IRCUT_ON
10	CIS Rst	O	U	CIS_RSTn for Sensor (with pull up resistor internal)
11	Day/Night	I	U	DAY/NIGHT Selection Default (with pull up resistor internal) 0 → Night (Black and White) 1 → Day (Colour)
	I2S_CLK	O		Multiplexing：I2S_CLK
12	CIS_SDA	I/O		I2C
13	CIS_SCL	I/O		
14	CVBS_HD_Sel0	I	U	HD_SEL0 Default (with pull up resistor internal)

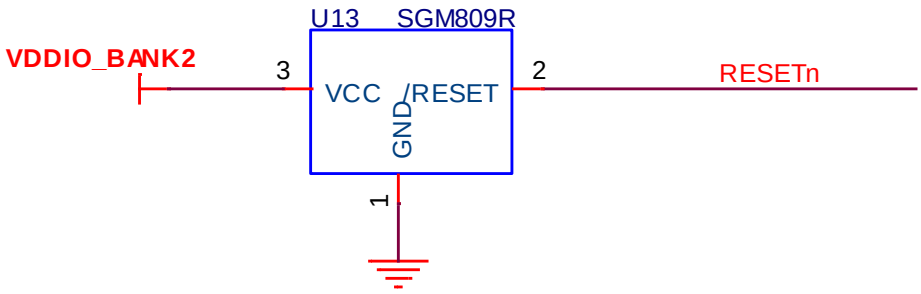
				｛HD_SEL1, HD_SEL0｝=00，CVBS output；Others HD outpur
	I2S_WS	O		Multiplexing：I2S_WS
15	CVBS_HD_Sel1			HD_SEL1 Default (with pull up resistor internal)
	I2S_TXD	O		Multiplexing：I2S_TXD
16	Fmt_Sel	I	U	FMT_SEL Default (with pull up resistor internal) CVBS : 0 → NTSC，1 → PAL HD: 0 → 30fps，1 → 25fps
	I2S_RXD	I	U	Multiplexing：I2S_RXD
17	PWM2	O	U	PWM2 (with pull up resistor internal)
	I2S_MCLK	O		Multiplexing：I2S_MCLK
	AVE_DEBUG	O		AVE debug for Test
18	SPI1_CS0	O	U	SPI1_CS0 (with pull up resistor internal)
	PWM3	O		Multiplexing：PWM3
19	SPI1_CS1	O	U	SPI1_CS1 (with pull up resistor internal)
	PWM4	O		Multiplexing：PWM4
20	SPI1_CLK	O	U	SPI1_CLK (with pull up resistor internal)
	PWM5	O		Multiplexing：PWM5
21	SPI1_TXD	O	U	SPI1_TXD (with pull up resistor internal)
	PWM6	O		Multiplexing：PWM6
22	SPI1_RXD	O	U	SPI1_RXD (with pull up resistor internal)
	PWM7	O		Multiplexing：PWM7
23	RX485_RX	I	U	RS485 Input
24	GPIO_24	O	D	GPIO
25	GPIO_25	O	D	GPIO
30	UART1_TX	O	U	UART1 TX
31	UART1_RX	I	U	UART1 RX

4.2 Reference Circuit

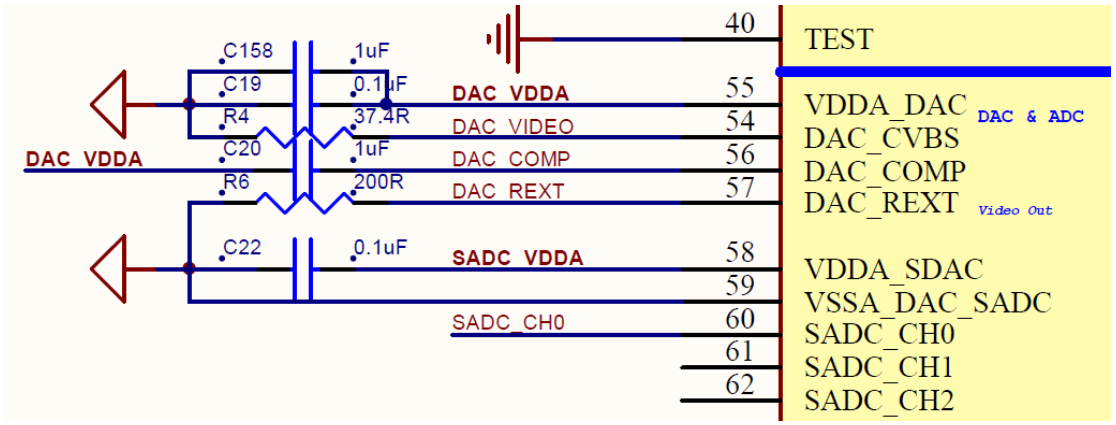
4.2.1 OSC Reference Circuit



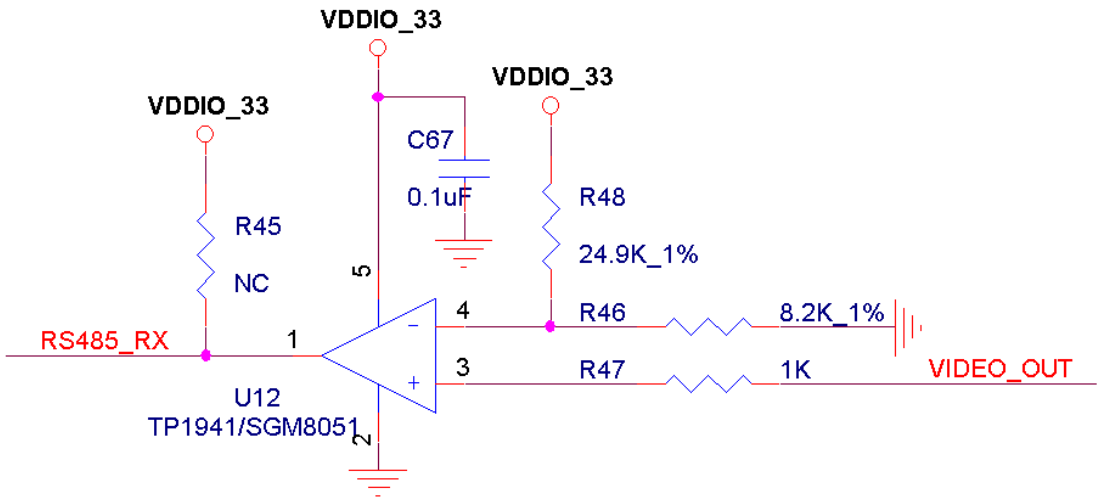
4.2.2 Reset Reference Circuit



4.2.3 DAC Reference Circuit



4.2.4 RS485 Reference Circuit



5. DC Electrical Specifications

5.1 Power Supply Specifications

Power Type	Description	Min	Type	Max	Unit
VDDK	Core Power	TBD	230	TBD	mA
DAC/ADC_VDDA	DAC/ADC Power	TBD	54	TBD	mA
VDDIO_BANK1	IO_BANK1 Power	TBD	1	TBD	mA
VDDIO_BANK2	IO_BANK2 Power	TBD	9	TBD	mA
DDRIO_18	DDR Power	TBD	56	TBD	mA

5.2 Working Conditions

Symbol	Parameter	Min	Type	Max	Unit
VDDK	Core Power	TBD	1.20	TBD	V
DAC/ADC_VDDA	DAC/ADC Power	TBD	3.30	TBD	V
VDDIO_BANK1	IO_BANK1 Power	TBD	3.30	TBD	V
		TBD	1.80	TBD	V

VDDIO_BANK2	IO_BANK2 Power	TBD	3.30	TBD	V
DDRIO_18	DDR Power	TBD	1.80	TBD	V

5.3 I/O Specifications

Symbol	Parameter	Min.	Norm	Max
VDD33	I/O supply voltage	2.97V	3.3V	3.63V
V_{IH}	Input High Voltage	2.0V		VDD33+0.3V
V_{IL}	Input Low Voltage	-0.3V		0.8V
V_T	Threshold point	1.30V	1.41V	1.53V
V_{T+}	Schmitt trig Low to High threshold point	1.54V	1.64V	1.74V
V_{T-}	Schmitt trig. High to Low threshold point	0.95V	1.02V	1.09V
T_J	Junction Temperature	0 ℃	25℃	125℃
I_L	Input Leakage Current			±1uA
I_{OZ}	Tri-State output leakage current			±1uA
R_{PU}	Pull-up Resistor	62kohm	77kohm	112kohm
R_{PD}	Pull-down Resistor	58kohm	81kohm	157kohm
V_{OL}	Output low voltage @I_{OL}=2,4…24mA			0.4V
V_{OH}	Output high voltage @ I_{OH}=2,4…24mA	2.4V		
I_{OL}	Low level output current @V_{OL}=0.4V			
	4mA	4.2mA	6.6mA	8.1mA
I_{OH}	High level output current @VOH=2.4V			
	4mA	4.7mA	9.6mA	14.9mA

Symbol	Parameter	Min.	Norm	Max
VDD33	I/O supply voltage	1.62V	1.8V	1.98V
V_{IH}	Input High Voltage	0.65* VDD33		VDD33+ 0.3V
V_{IL}	Input Low Voltage	-0.3V		0.35* VDD33
V_T	Threshold point	0.76V	0.82V	0.87V
V_{T+}	Schmitt trig Low to High threshold point	0.95V	1.04V	1.09V
V_{T-}	Schmitt trig. High to Low threshold point	0.55V	0.59V	0.62V
T_J	Junction Temperature	0 ℃	25℃	125℃
I_L	Input Leakage Current			±1uA
I_{OZ}	Tri-State output leakage current			±1uA
R_{PU}	Pull-up Resistor	123kohm	174kohm	276kohm
R_{PD}	Pull-down Resistor	126kohm	202kohm	416kohm
V_{OL}	Output low voltage @I_{OL}=2,4…24mA			0.45V
V_{OH}	Output high voltage @ I_{OH}=2,4…24mA	VDD33-0.45V		
I_{OL}	Low level output current @V_{OL}=0.45V			
	4mA	2.0mA	3.7mA	5.3mA
I_{OH}	High level output current @VOH=VDD33-0.45V			
	4mA	1.8mA	3.0mA	4.2mA

5.4 Power up Sequence

The digital and analog supply voltages can be powered in any order, on the basis of system reset time keep TBD ms at least.

5.5 PLL Specifications

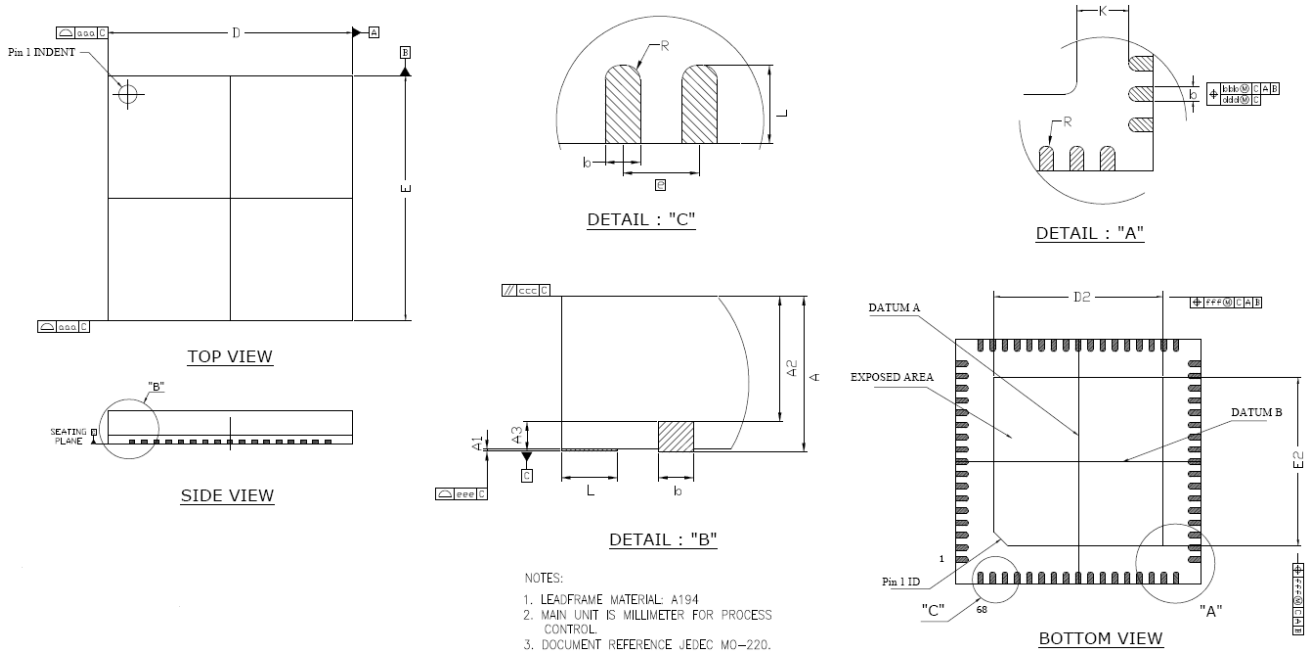
Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input clock frequency	XIN/N	1	-	50	MHz	
VCO frequency	VOUT	500	-	1500	MHz	
Output clock frequency	CLK_OUT	62.5	-	1500	MHz	
Period jitter	RMS	-	12	-	ps	VCO freq = 960 MHz; Clean Power Temp=25℃,TT,1.2V
	PK_PK	-	80	-	ps	
Duty cycle	--	40	50	60	%	VCO freq = 500 ~1500 MHz

6. Temperature Specifications

FH8550M Operating Temperature: -20℃～+70℃。

7. Package

The chip package is QFN68. Its body size is 8.00mm x 8.00mm x 0.85mm. The following figure shows the package and the dimensions of the FH8550M.



Dimension Matrix:

SYMBOL: \ UNIT & DIMENSION:	DIMENSION UNIT:MM		
	MIN	NOM	MAX
e (LEAD PITCH):		0.400 BSC	
D,E (PKG SIZE):	7.900	8.000	8.100
D1,E1 (CAVITY WIDTH(X)):		--	
L (LEAD LENGTH):	0.350	0.400	0.450
N (LEAD COUNT):	--	68.000	--
A (OVERALL HEIGHT):	0.800	0.850	0.900
A1 (STANDOFF):	--	--	0.050
A2 (MOLD HEIGHT):	--	0.650	--
A3 (L/F THICKNESS):		0.203 REF	
R (LEAD R-FILLET):	--	0.075	--
b (LEAD WIDTH):	0.150	0.200	0.250
K (TIP TO EXPOSED PAD EDGE):	0.200	--	--
θ (DRAFT ANGLE):	--	--	--

TOLERANCE OF FORM & POSITION: UNIT: MM			
	MIN	NOM	MAX
aaa	--	--	0.100
bbb	--	--	0.070
ccc	--	--	0.200
ddd	--	--	0.050
eee	--	--	0.080
fff	--	--	0.100

L/F	D2 , E2 (EXPOSED PAD SIZE): DIMENSION UNIT:MM		
	MIN	NOM	MAX
(1.)	5.400	5.500	5.600

8. Boot Select

The following table provides three boot modes which FH8550M supports. It depends on the status of GPIO_2 and GPIO_3 during power up stage.

Table 2 Boot Select

GPIO	GPIO_3=0	GPIO_3=1
GPIO_2=0	SPI Master Mode	Xmodem Mode
GPIO_2=1	SPI Slave Mode	Xmodem Mode

- SPI Master mode: normal work, boot from SPI Flash.
- SPI Slave mode: work as SPI slave mode.
- Xmodem mode: update mode, down the code from PC to SPI Flash or DDR by UART0.