H9G4750M10P

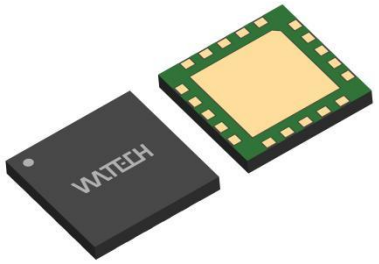
10W, 4.7 - 5.0 GHz LDMOS MMIC Amplifier

Product datasheet

Description

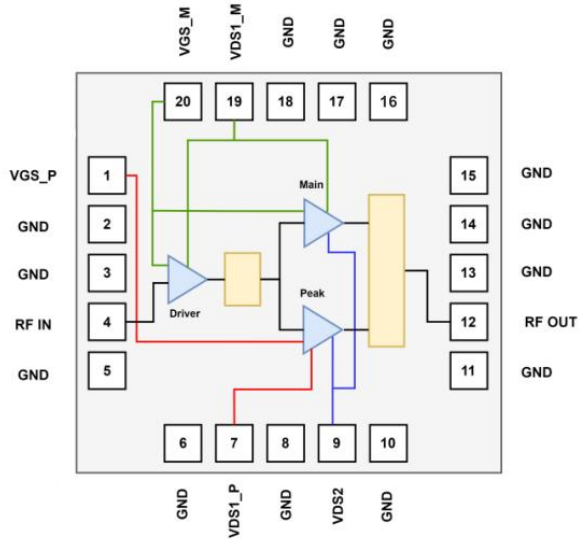
The H9G4750M10P is a LDMOS MMIC Integrated Asymmetrical Doherty based on 2-Stage with 10W saturated output power covering frequency range from 4.7 - 5.0 GHz.

The amplifier is 50 Ω Input/Output matched with a small compact footprint 7x7 mm which makes it ideal for integration.



20 Pin LGA 7x7 mm Plastic Package

Block Diagram



H9G4750M10P Block Diagram

Features

- Operating Frequency Range: 4.7 - 5.0 GHz
- Operating Drain Voltage: +22V
- Saturation Output Power: 10W
- Power Average: 0.6W
- 50 Ω Input/Output matched
- Integrated Input Divider
- Integrated Output Combiner
- Integrated Asymmetrical Doherty Final Stage
- High Efficiency: 20.7%@4.85GHz, WCDMA
- High Gain: 33.9dB@4.85GHz, WCDMA
- Small footprint package: LGA 7x7 mm

Applications

- 3GPP 5G NR FR1 n79
- Power Amplifier for Small Cells
- Driver Amplifier for Micro and Macro Base Stations
- Active Antenna Array for 5G mMIMO
- Repeaters/DAS
- Mobile Infrastructure

Ordering Information

Part Number	Description
H9G4750M10P	Reel Package
H9G4750M10PEVB	4.7 - 5.0 GHz EVB

Typical Performance

RF Characteristics (Pulsed CW)

Freq (GHz)	P3dB (dBm)	Gain (dB)	Eff (%)	IRL (dB)
4.700	40.6	33.7	21.3	18
4.850	40.7	33.8	20.1	14
5.000	40.7	33.8	20.0	15

Test conditions unless otherwise noted: 25 °C, V_{DD} = +22Vdc, I_{DQ} = 42mA, Vgsp = Vgsm-0.45V, Pulse Width = 100us, Duty Cycle = 10% test on HOTLO Application Board

RF Characteristics (WCDMA)

Freq (GHz)	Gain (dB)	Eff (%)	IRL (dB)	ACPR* @5MHz (dBc)	ACPR* @10MHz (dBc)
4.700	33.8	21.5	18	-32.2	-51
4.850	33.9	20.7	14	-34.7	-52
5.000	33.8	20.7	15	-34.7	-52

Test conditions unless otherwise noted: 25 °C, V_{DD}=+22Vdc, I_{DQ} = 42mA, Vgsp = Vgsm-0.45V, PAVG = 28 dBm
1C-WCDMA 5MHz Signal, 7.6 dB PAR @ 0.01% CCDF test on HOTLO Application Board
**Uncorrected DPD*

Absolute Maximum Ratings

Parameter	Range/Value	Unit
Drain voltage (V_{DSS})	-0.5 to +65	V
Gate voltage (V_{GS})	-5 to +10	V
Drain voltage (V_{DD})	0 to +28	V
Storage Temperature (T_{STG})	-55 to +150	°C
Case Temperature (T_C)	-40 to +125	°C
Junction Temperature (T_J)	-40 to +175	°C
Maximum Input Power (P_{IN})	10	dBm

Electrical Specification

DC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Breakdown Voltage $V_{(BR)DSS}$	Vgs=0V, Ids=100uA	65	-	-	V
Gate-Source Threshold Voltage $V_{GS(th)}$	Vgs=Vds, Ids=5.2uA	1.2	-	2.0	V
Drain Leakage Current I_{DSS}	Vgs=0V, Vds=28V	-	-	0.5	uA
Gate Leakage Current I_{GSS}	Vgs=5V, Vds=0V	-	-	0.05	uA

RF Characteristics (Pulsed CW)

Parameter	Freq (GHz)	Min	Typ.	Max	Unit
P3dB	5.000	40	40.5	-	dBm

Test conditions unless otherwise noted: 25 °C, V_{DD} = +22Vdc, I_{DQ} = 42mA, Vgsp = Vgsm-0.45V, Pulse Width = 100us, Duty Cycle = 10% test on HOTLO Production Board

RF Characteristics (WCDMA)

Parameter	Conditions	Min	Typ.	Max	Unit
Frequency	5.000				GHz
Gain	P_{AVG} = 28 dBm	31	33	36	dB
Eff	P_{AVG} = 28 dBm	18	20	-	%
IRL	P_{AVG} = 28 dBm	10	15	-	dB
ACPR@5MHz*	P_{AVG} = 28 dBm	-	-34	-30	dBc

Test conditions unless otherwise noted: 25 °C, V_{DD}=+22Vdc, I_{DQ} = 42mA, Vgsp = Vgsm-0.45V, 1C-WCDMA 5MHz Signal, 7.6 dB PAR @ 0.01% CCDF test on HOTLO Production Board

**Uncorrected DPD*

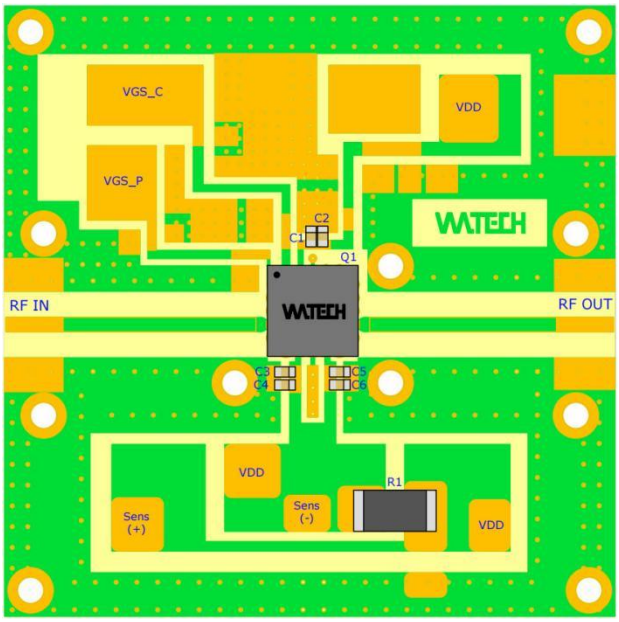
Load Mismatch Test

Condition	Test Result
VSWR=10:1, at all Phase Angles, V_{DD}=+22Vdc, I_{DQ} = 42 mA, Vgsp=Vgsm-0.45V, P_{AVG} = 28 dBm, Frequency 4.500 - 5.000 GHz test on HOTLO Application Board	No Device Degradation

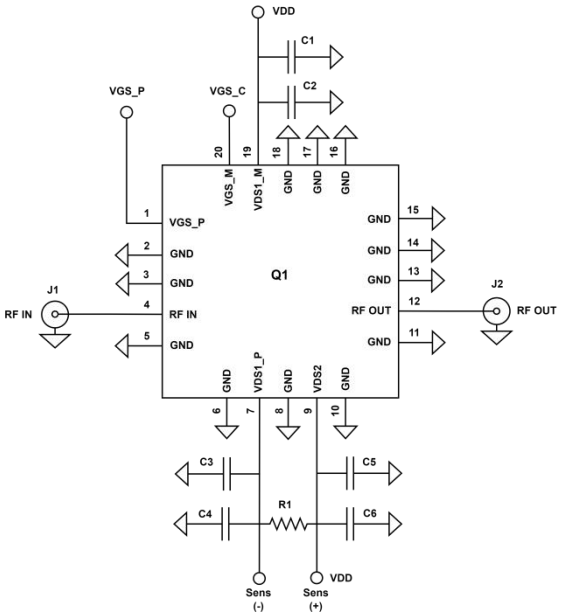
Thermal Information

Parameter	Condition	Value (Typ)	Unit
Thermal Resistance Junction to Case (R_{TH})	T_{CASE}= 90°C, 1C-WCDMA 5MHz Signal, 7.6 dB PAR, P_{AVG} = 28 dBm	9.5	°C /W

H9G4750M10P 4.7 - 5.0 GHz Reference Design (47 x47 mm)



EVB Layout

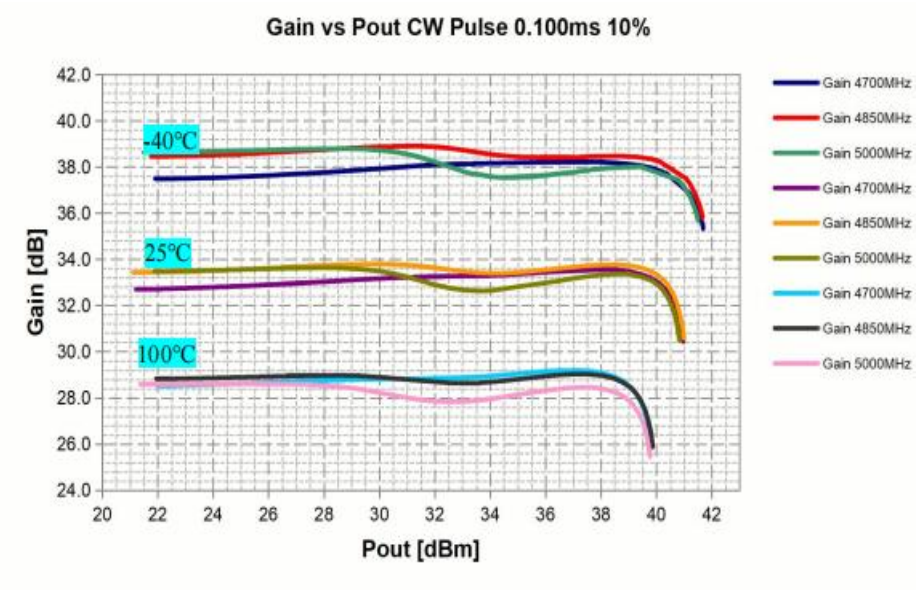


EVB Schematic

Bill of Materials (BoM) - H9G4750M10P 4.7 - 5.0 GHz Reference Design

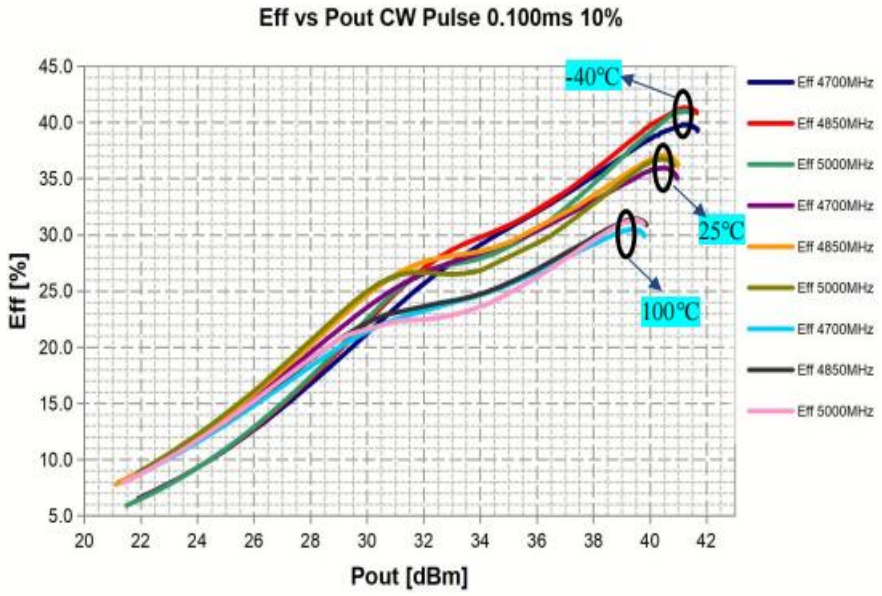
Reference	Value	Description	Manufacturer	P/N
Q1	-	10W, 3.3 3.6 GHz LDMOS MMIC PA	Holto	H9G4750M10P
C1, C3, C5	1uF ±10%, 0603	Multi-Layer Ceramic Capacitor	Murata	GCM188R71E105KA64D
C2, C4, C6	10uF ±20%, 0603	Multi-Layer Ceramic Capacitor	Murata	GRM188R6YA106MA73J
R1	100mΩ/1W, 0.1%	High-Precision Resistor	Vishay	Y44870R10000B0R
PCB	• Rogers 4350B, er = 3.66; Thickness= 20 mil (0.508 mm); Thickness copper plating = 35 µm (1oz) • Soldered on a 47x47x10 mm Copper Base-Plate			

Performance Plots



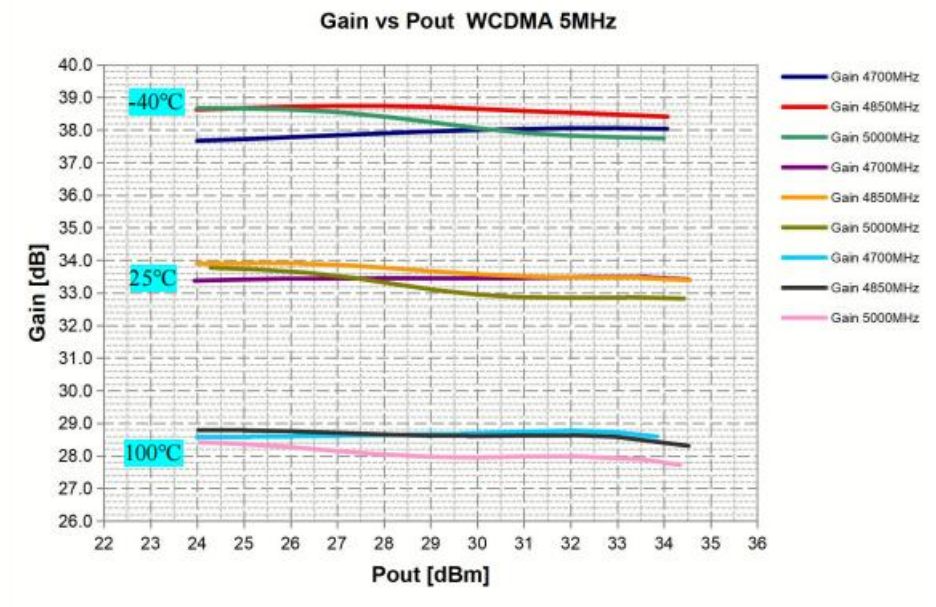
Pulsed CW, Gain and Efficiency vs Pout

Test conditions unless otherwise noted: 25 °C, V_{DD} = +22Vdc, I_{DQ} = 42mA, Vgsp = Vgsm-0.45V, Pulse Width = 100 us, Duty Cycle = 10% test on HOTLO Application Board



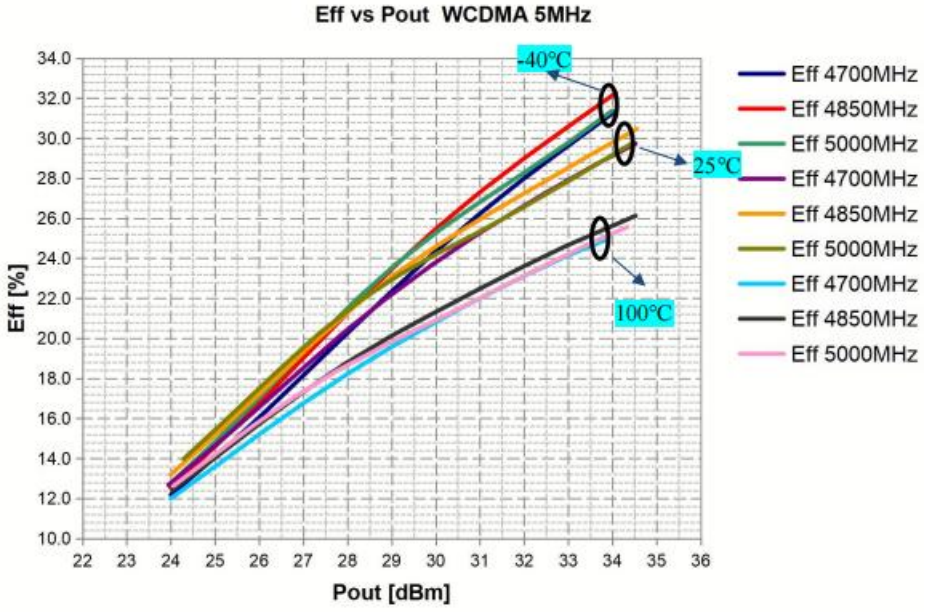
WCDMA, Gain and Efficiency vs Pout

Test conditions unless otherwise noted: 25 °C, V_{DD}=+22Vdc, I_{DQ} = 42mA, Vgsp = Vgsm-0.45V, 1C-WCDMA 5MHz Signal, 7.6 dB PAR @ 0.01% CCDF test on HOTLO Application Board



WCDMA, ACPR_5MHz, ACPR_10MHzvs Pout

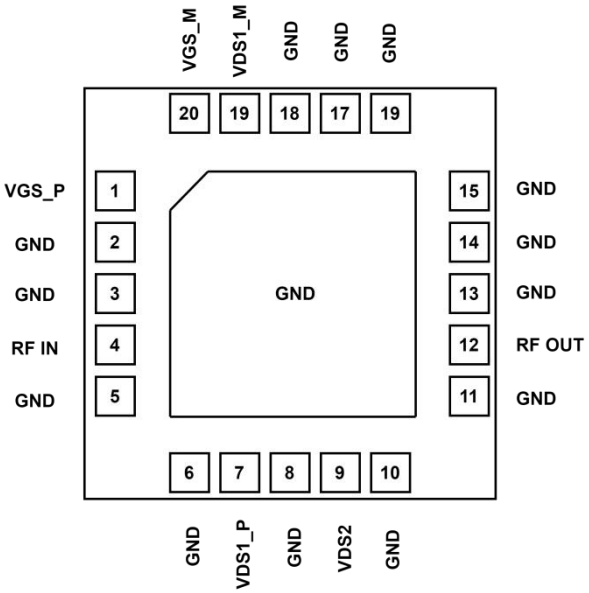
Test conditions unless otherwise noted: 25 °C, V_{DD}=+22Vdc, I_{DQ} = 42mA, Vgsp = Vgsm-0.45V, 1C-WCDMA 5MHz Signal, 7.6 dB PAR @ 0.01% CCDF test on HOTLO Application Board



WCDMA, ACPR_5MHz, ACPR_10MHzvs Pout

Test conditions unless otherwise noted: 25 °C, V_{DD}=+22Vdc, I_{DQ} = 42mA, Vgsp = Vgsm-0.45V, 1C-WCDMA 5MHz Signal, 7.6 dB PAR @ 0.01% CCDF test on HOTLO Application Board

Pin Configuration and Description



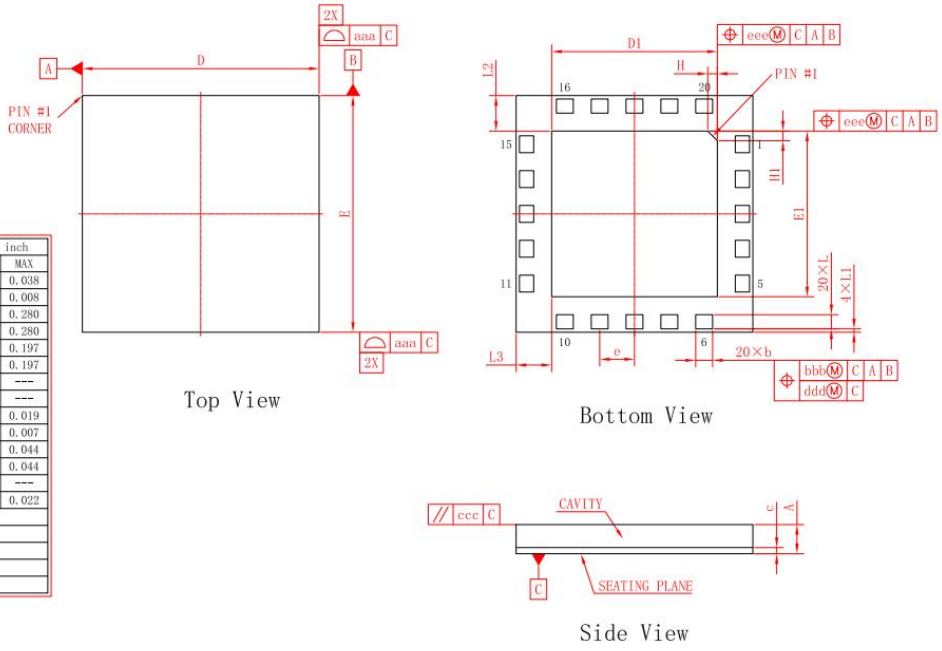
Pinout Device Configuration

Pin Number	Label	Description
1	VGS_P	Gate-Source Voltage Peak
2	GND	Ground
3	GND	Ground
4	RFIN	RF Input
5	GND	Ground
6	GND	Ground
7	VDS1_P	Drain-Source Voltage Peak Driver
8	GND	Ground
9	VDS2	Drain-Source Voltage Final Stage
10	GND	Ground
11	GND	Ground
12	RFOUT	RF Output
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	GND	Ground
18	GND	Ground
19	VDS1_M	Drain-Source Voltage Main Driver
20	VGS_M	Gate-Source Voltage Main

Package Marking and Dimensions

- LIne1 (fixed): Device name in W/O
- Line2 (unfixed): Marking Lot No in W/O (Sample: E596-20140001)
- Line3 (unfixed): Date Code + JY
- This Marking SPEC only stipulates the content of Marking. For marking requirements such as font and size, please refer to the latest version of "Holto Product Printing Specification"

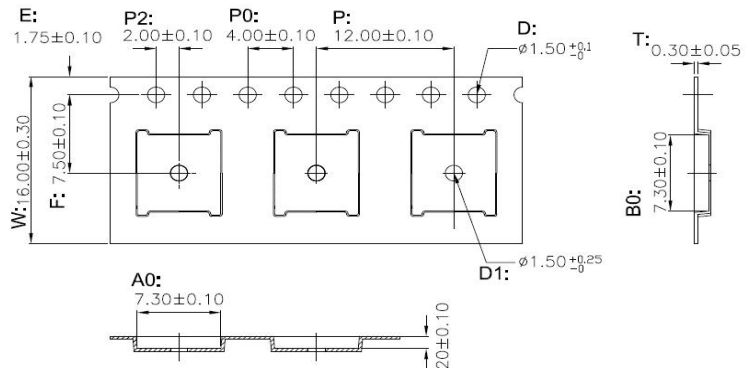
Marking



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.760	0.860	0.960	0.030	0.034	0.038
c	0.150	0.180	0.210	0.006	0.007	0.008
D	6.900	7.000	7.100	0.272	0.276	0.280
E	6.900	7.000	7.100	0.272	0.276	0.280
D1	4.800	4.900	5.000	0.189	0.193	0.197
E1	4.800	4.900	5.000	0.189	0.193	0.197
H	---	0.286	---	---	0.011	---
H1	---	0.286	---	---	0.011	---
L	0.370	0.420	0.470	0.015	0.017	0.019
L1	0.025	0.100	0.175	0.001	0.004	0.007
L2	0.975	1.050	1.125	0.038	0.041	0.044
L3	0.975	1.050	1.125	0.038	0.041	0.044
e	---	1.030	---	---	0.041	---
b	0.450	0.500	0.550	0.018	0.020	0.022
aaa	0.150			0.006		
bbb	0.150			0.006		
ccc	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		

Package Dimensions

Tape and Reel Information



Notes:

1. Carrier tape color: BLACK.
2. Carrier material :PS (Polystyrene).
3. ESD surface resistivity < 1× 1011 Ω/square per EJA, JEDEC TNR specification.
4. Heat deflection temperature for Tape & Reel material: 62°C
5. Vicat softening temperature (10N) for Tape & Reel material: 95°C
6. Dimension is millimeter.

Tape & Reel Packaging Descriptions

Reflow information

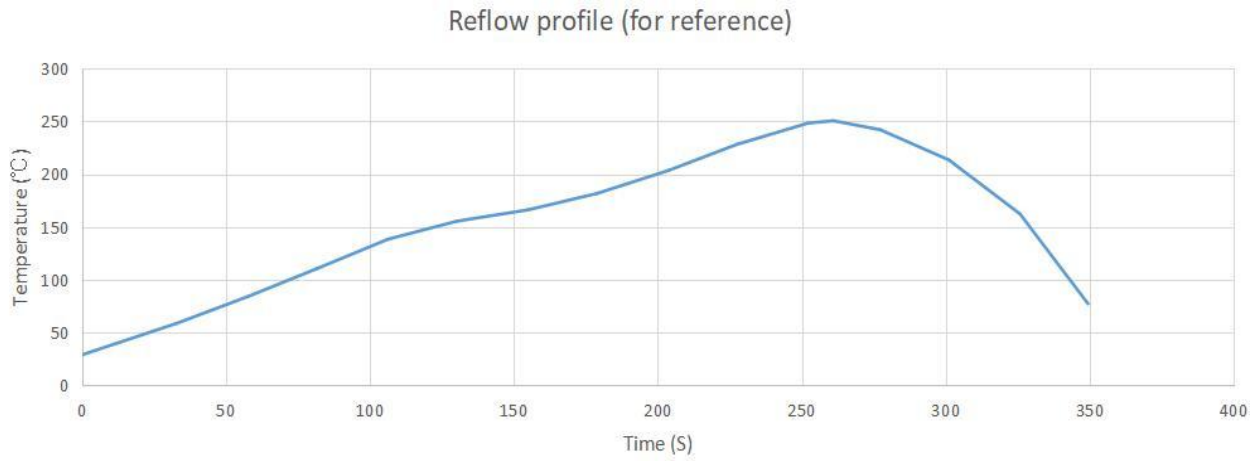
Reflow Profile classification (JEDEC JSTD020E-lead free)

Profile Feature	Classification	Units	Remark
Ramp-up rate (Max)	3	°C /second	
Dwell temperature	150~200	°C	
Dwell time	60~120	second	SAC Liquid is 217 °C
Time above liquid	60~150	second	
Peak temperature	255~260	°C /second	
Peak soak time	30*	second	* Tolerance for peak profile temp erature is defined as a supplier mi nimum and a user maximum.
Ramp-down rate (Max)	6	°C /second	
Time 25℃ to peak temperature(Max)	8	minutes	

Reflow Oven Settings (reference)

Belt Speed	Zone #1	Zone #2	Zone #3	Zone #4	Zone #5	Zone #6	Zone #7	Zone #8	Zone #9	Zone #10
75cm/min	85	110	135	160	170	175	200	240	250	260

Reflow Oven Settings (reference)



Reflow Profile

Handling Precautions

Parameter	Grade
Moisture Sensitivity Level MSL	3

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	JESD22-A114
ESD – Human Body Model (MM)	Class A	EIA/JESD22-A115
ESD – Charged Device Model (CDM)	Class III	JESD22-C101

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

Datasheet Status

Document status	Product status	Definition
Objective Datasheet	Design simulation	Product objective specification
Preliminary Datasheet	Customer sample	Engineering samples and first test results
Product Datasheet	Mass production	Final product specification

Abbreviations

Acronym	Definition
LDMOS	Laterally-Diffused Metal-Oxide Semiconductor
CW	Continuous Waveform
VSWR	Voltage Standing Wave Ratio

Revision history

Document ID	Datasheet Status	Release Date	Revision Version
Rev 1.0	Product	Dec 2021	Product release
Rev 1.1	Product	Jan 2022	Add maximum Input Power in Absolute Maximum Ratings table
Rev 1.2	Product	March 2023	New format based on English version datasheet

Contact Information

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