HT647P(B)

200W, 600 - 1600 MHz LDMOS Amplifier

Product datasheet

Description

The HT647P(B) is an unmatched discrete LDMOS Power Amplifier with 200W saturated output power covering frequency range from 600 - 1600 MHz.

Features

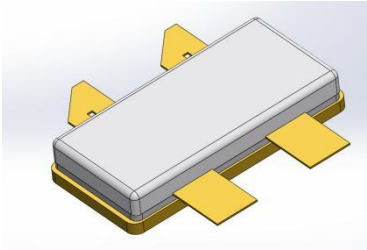
- Operating Frequency Range: 600 - 1600 MHz
- Operating Drain Voltage: 20-28V
- Saturation Output Power: 200W
- Device can be used on a single-ended or in a push-pull configuration.
- Excellent thermal stability due to low thermal resistance package
- Enhanced robustness design without device degradation

Applications

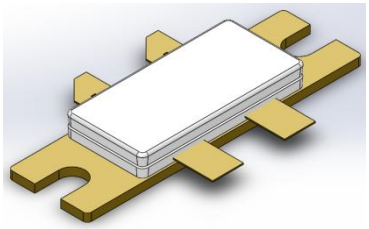
- Industrial, scientific, medical (ISM)
  - Laser generation
  - Plasma generation
  - Particle accelerators
  - MRI, RF ablation and skin treatment
  - Industrial heating, welding and drying systems

Ordering Information

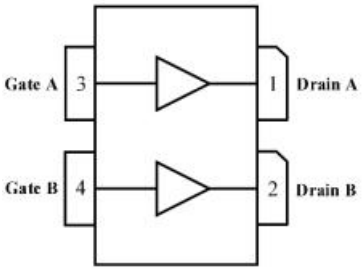
Part Number	Description
HT647P(B)	Tray Package
HT647P(B)EVB	600 MHz EVB
HT647P(B)EVB1	1300 MHz EVB
HT647P(B)EVB2	1350 - 1400 MHz EVB



ACC2110S-4L
Earless Flanged balanced
Air Cavity Ceramic Package; 4 Leads
HT647P



ACC2110B-4L
Flanged balanced
Air Cavity Ceramic Package; 4 Leads,
2 Mounting holes
HT647PB



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor

Pin Connections

Typical Performance

RF Characteristics (CW, class AB)

Freq (MHz)	P1dB (dBm)	P1dB (W)	Gain (dB)	Eff (%)
1350	53	200	19.6	59

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ = 600mA CW test on HOTLO Application Board

RF Characteristics (Pulsed CW ,class AB)

Freq (MHz)	P1dB (dBm)	P1dB (W)	Gain (dB)	Eff (%)
1350	53.4	220	19.7	61

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ = 600mA, PW = 100us, DC= 10% test on HOTLO Application Board

Absolute Maximum Ratings

Parameter	Range/Value	Unit
Drain voltage (V_{DSS})	-0.5 to +65	V
Gate voltage (V_{GS})	-5 to +10	V
Storage Temperature (T_{STG})	-55 to +150	°C
Junction Temperature (T_J)	-40 to +225	°C

Electrical Specification

DC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Breakdown Voltage $V_{(BR)DSS}$	Vgs=0V, Ids=108uA	65	-	-	V
Gate-Source Threshold Voltage $V_{GS(th)}$	Vds=Vgs, Ids=108uA	-	1.5	-	V
Drain Leakage Current I_{DSS}	Vgs=0V, Vds=65V	-	-	10	uA
Gate Leakage Current I_{GSS}	Vgs=5V, Vds=0V	-	-	1	uA
Drain-Source On Resistance $R_{DS(on)}$	Vgs=10V, Ids=540mA	-	100	-	mΩ

Load Mismatch Test

Condition	Test Result
VSWR=10:1 at all Phase Angles, VDD = +28Vdc, IDQ= 600mA, P_{AVG} = 53 dBm (200W), CW signal @1300 MHz	No Device Degradation

Thermal Information

Parameter	Condition	Value (Typ)	Unit
Thermal Resistance Junction to Case (R_{TH})	T_{CASE}= 80°C, VDD = +28Vdc, IDQ= 600mA, P_{AVG} = 53 dBm (200W), CW signal	0.4	°C /W

Load Pull Performance

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 600mA, PW = 40us, DC= 4%

Max Output Power						
Freq (MHz)	Z_source (Ω)	Z_load [1] (Ω)	Gain (dB)	P1dB (dBm)	P1dB (W)	Eff (%)
1200	0.56-j*1.71	1.01-j*2.01	19.8	53.9	245	59.7
1300	0.65-j*1.85	0.81-j*2.10	21.2	53.5	224	58.9
1400	1.28-*j2.23	0.65-j*2.25	22.2	53.2	209	56.5
1600	0.47-j*1.19	0.96-j*2.73	22.2	52.9	195	52.4

[1] Load impedance for optimum P1dB pout

Max Output Power						
Freq (MHz)	Z_source (Ω)	Z_load [2] (Ω)	Gain (dB)	P3dB (dBm)	P3dB (W)	Eff (%)
1200	0.56-j*1.71	1.13-j*2.26	19.1	54.7	295	61.7
1300	0.65-j*1.85	0.81-j*2.16	21.1	54.2	263	61.2
1400	1.28-*j2.23	0.95-j*2.44	22.3	54.0	251	58.3
1600	0.47-j*1.19	1.07-j*2.78	22.1	54.0	251	55.6

[2] Load impedance for optimum P3dB pout

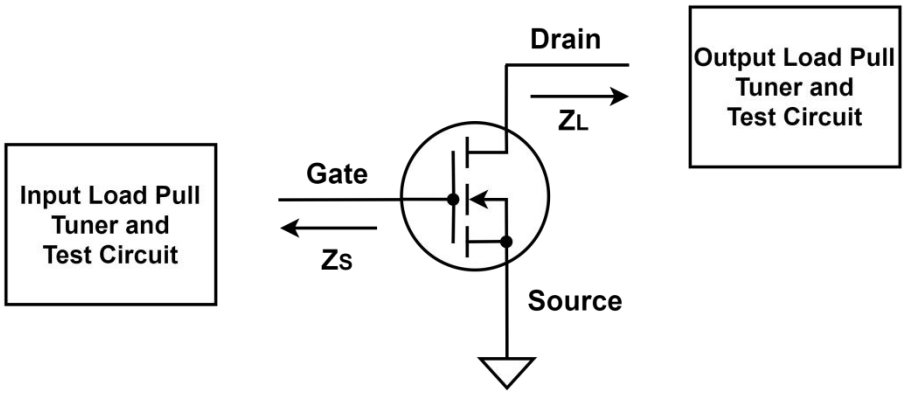
Max Drain Efficiency						
Freq (MHz)	Z_source (Ω)	Z_load [3] (Ω)	Gain (dB)	P1dB (dBm)	P1dB (W)	Eff (%)
1200	0.56-j*1.71	0.90-j*1.15	23.7	52.3	170	71.2
1300	0.65-j*1.85	0.78-j*1.37	25.9	51.5	141	68.2

1400	1.28-j*2.23	0.85-j*1.64	26.4	51.5	141	65.6
1600	0.47-j*1.19	0.56-j*2.05	25.7	51.5	141	64.2

[3] Load impedance for optimum P1dB efficiency

Max Drain Efficiency						
Freq (MHz)	**Z_source (Ω)**	**Z_load [4] (Ω)**	**Gain (dB)**	**P3dB (dBm)**	**P3dB (W)**	**Eff (%)**
1200	0.56-j*1.71	1.12-j*1.50	22.3	53.9	254	72.3
1300	0.65-j*1.85	1.01-j*1.58	24.5	53.0	200	70.3
1400	1.28-j*2.23	0.84-j*1.86	25.7	53.0	200	67.7
1600	0.47-j*1.19	0.63-j*2.01	25.7	52.1	162	66.2

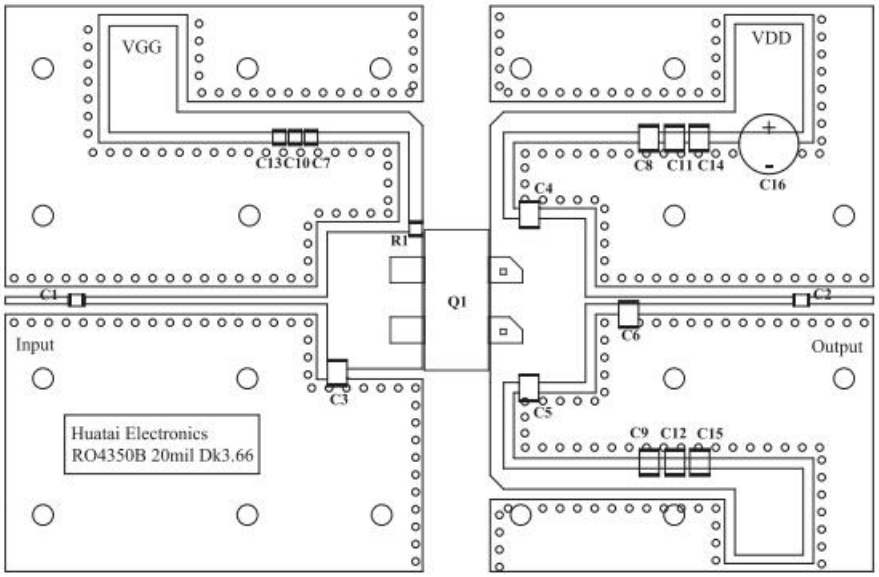
[4] Load impedance for optimum P3dB efficiency



Z_source : Measured impedance presented to the input of the device at the package reference plane

Z_load : Measured impedance presented to the output of the device at the package reference plane

HT647P(B) 1300 MHz Reference Design

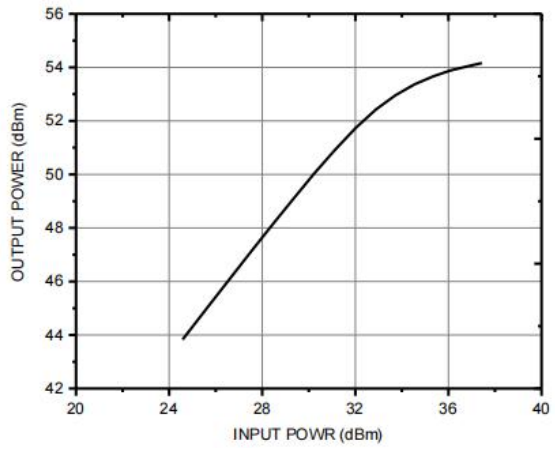


EVB Layout

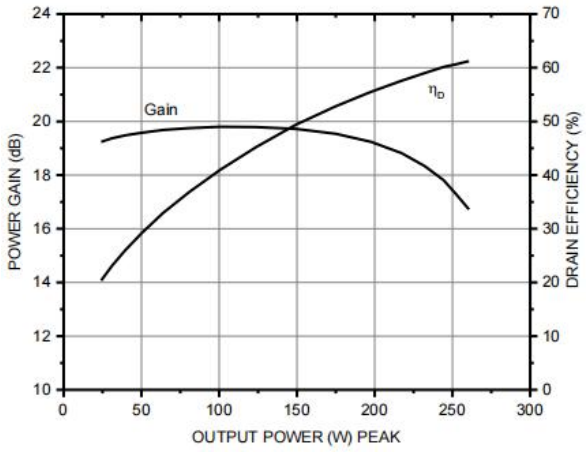
Bill of Materials (BoM) - HT647P(B) 1300 MHz Reference Design

Reference	Value	Description	Manufacturer	P/N
Q1	-	200W, 600 - 1600 MHz LDMOS PA	Holto	HT647P(B)
C1	200pF	MLCC	Murata	GRM2165C1H201JA01D
C2	18pF	MLCC	KEMET	CBR08C180FAGAC
C3, C4, C5	5.6pF	MLCC	ATC	ATC100B5R6JT500XT
C6	3.3pF	MLCC	ATC	ATC100B3R3JT500XT
C7, C8, C9	30pF	MLCC	Samsung	CL31C300JBCNNNC
C10, C11, C12	1nF	MLCC	ATC	800B102JT50XT
C13	4.7uF	MLCC	Murata	GRM31CR71H475KA12L
C14, C15	1uF	MLCC	Murata	GRM31CR41H105KA61L
C16	470uF	Electrolytic Capacitor	Vishay	MAL203859471E3
R1	51Ω	Thick Film Resistor	YAGEO	RC0603FR-0751RL
PCB	Rogers 4350B (er = 3.66), 20 mil (0.508 mm), 35 µm (1oz)			

Performance Plots

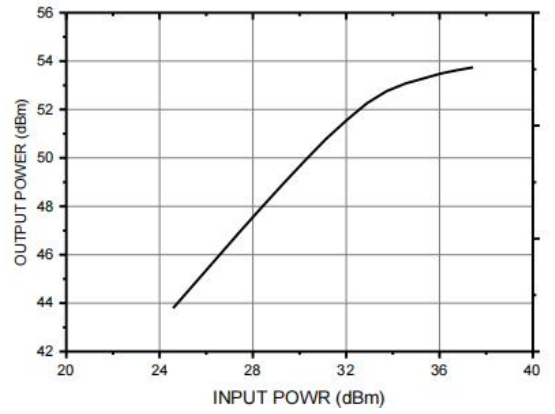


Pulsed CW, Pout vs Pin

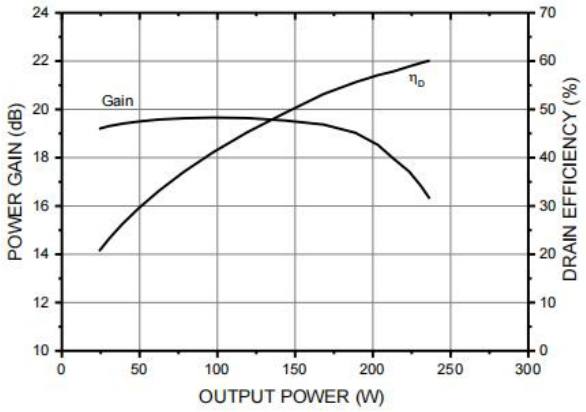


Pulsed CW, Gain and Efficiency vs Pout

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 600mA, PW = 100us, DC= 10% test on HOTLO Application Board



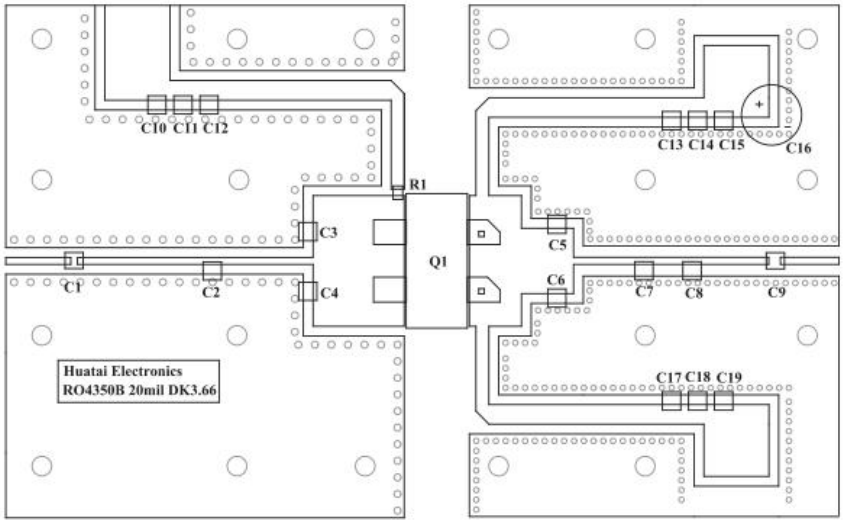
CW, Pout vs Pin



CW, Gain and Efficiency vs Pout

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 600mA test on HOTLO Application Board

HT647P(B) 600 MHz Reference Design

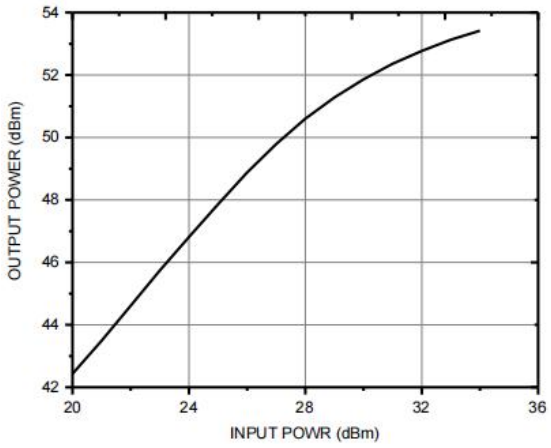


EVB Layout

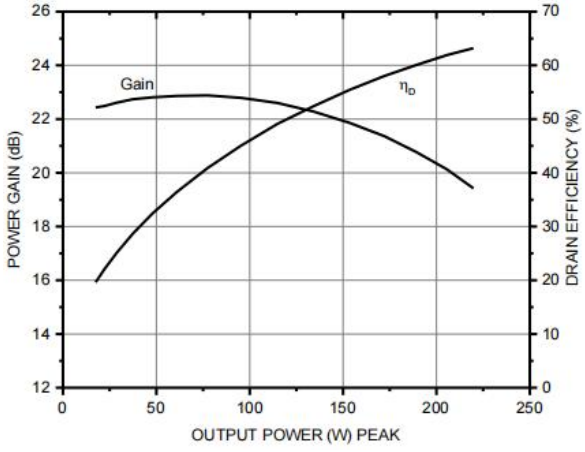
Bill of Materials (BoM) - HT647P(B) 600 MHz Reference Design

Reference	Value	Description	Manufacturer	P/N
Q1	-	200W, 600 - 1600 MHz LDMOS PA	Holto	HT647P(B)
C1, C9, C12, C13, C17	180pF	MLCC	ATC	ATC100B181JT500XT
C2	4.7pF	MLCC	ATC	ATC100B4R7JT500XT
C3	33pF	MLCC	ATC	ATC100B330JT500XT
C4	36pF	MLCC	ATC	ATC100B360JT500XT
C5, C6	20pF	MLCC	ATC	ATC100B200JT500XT
C7	12pF	MLCC	ATC	ATC100B120JT500XT
C8	3.6pF	MLCC	ATC	ATC100B3R6JT500XT
C10, C15, C19	1uF	MLCC	Murata	GRM31CR41H105KA61L
C11, C14, C18	1nF	MLCC	ATC	800B102JT50XT
C16	470uF	Electrolytic Capacitor	Vishay	MAL203859471E3
R1	10Ω	Thick Film Resistor	YAGEO	RC0603FR-0710RL
PCB	Rogers 4350B (er = 3.66), 20 mil (0.508 mm), 35 µm (1oz)			

Performance Plots

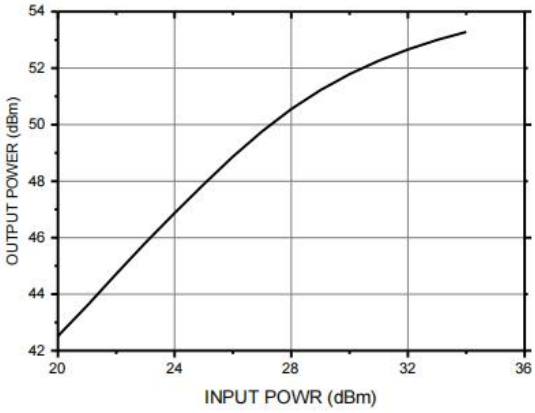


Pulsed CW, Pout vs Pin

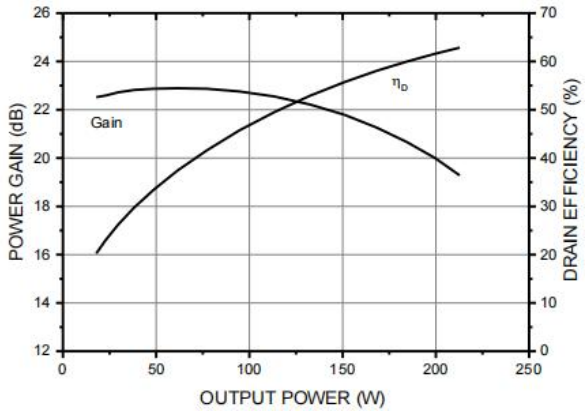


Pulsed CW, Gain and Efficiency vs Pout

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 600mA, PW = 100us, DC= 10% test on HOTLO Application Board



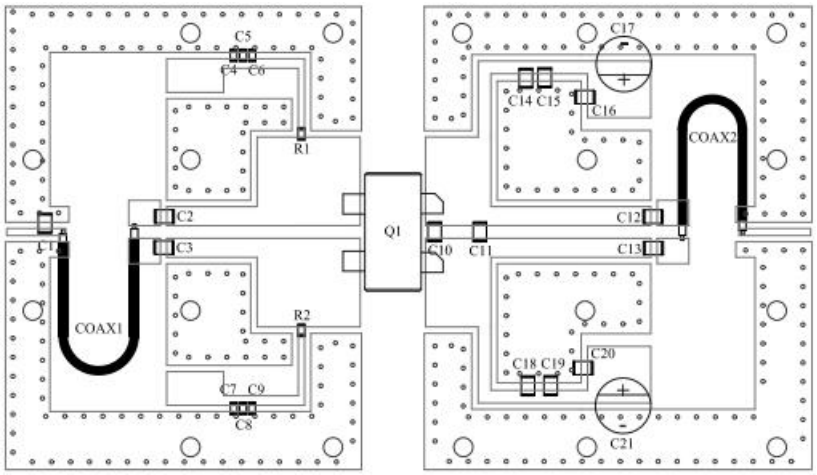
CW, Pout vs Pin



CW, Gain and Efficiency vs Pout

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 600mA test on HOTLO Application Board

HT647P(B) 1350 - 1400 MHz Reference Design

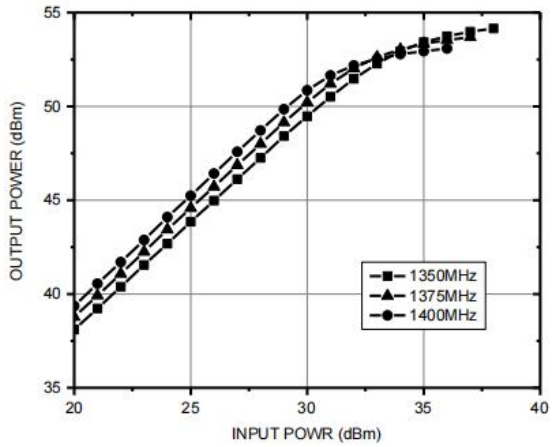


EVB Layout

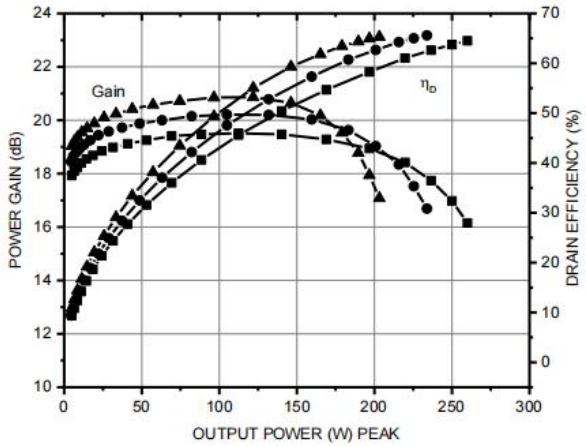
Bill of Materials (BoM) - HT647P(B) 1350 - 1400 MHz Reference Design

Reference	Value	Description	Manufacturer	P/N
Q1	-	200W, 600 - 1600 MHz LDMOS PA	Holto	HT647P(B)
C2, C3, C12, C13, C14, C18	39pF	MLCC	ATC	ATC100B390JT500XT
C1	2pF	MLCC	ATC	ATC100B2R0JT500XT
C10	4.3pF	MLCC	ATC	ATC100B4R3JT500XT
C11	2.7pF	MLCC	ATC	ATC100B2R7JT500XT
C15, C19	1nF	MLCC	ATC	800B102JT50XT
C6, C9	39pF	MLCC	ATC	600S390BT260XT
C5, C8	1nF	MLCC	Murata	GRM1885C1H102JA01
C4, C7	1uF	MLCC	Murata	GRM31CR41H105KA61L
C16, C20	10uF	MLCC	Murata	GRJ32ER71H106KE11L
C17, C21	470uF	Electrolytic Capacitor	Vishay	MAL203859471E3
R1, R2	10Ω	Thick Film Resistor	YAGEO	RC0603FR-0710RL
PCB	Rogers 4350B (er = 3.66), 20 mil (0.508 mm), 35 µm (1oz)			

Performance Plots

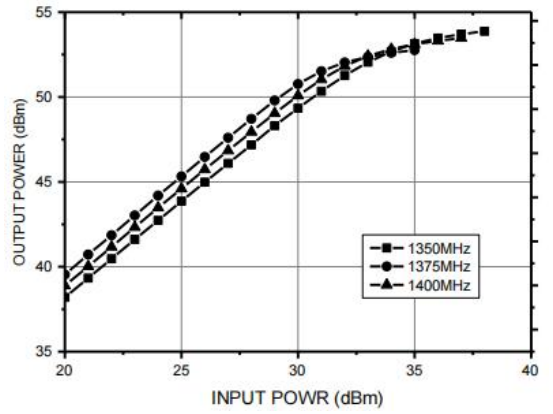


Pulsed CW, Pout vs Pin

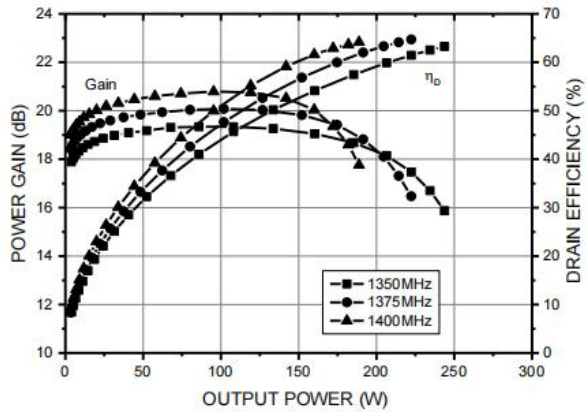


Pulsed CW, Gain and Efficiency vs Pout

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 600mA, PW = 100us, DC= 10% test on HOTLO Application Board



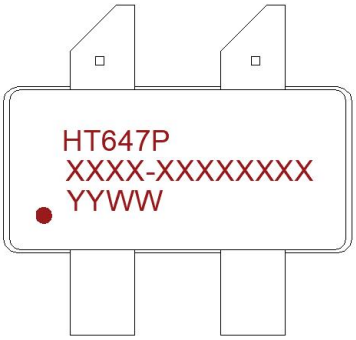
CW, Pout vs Pin

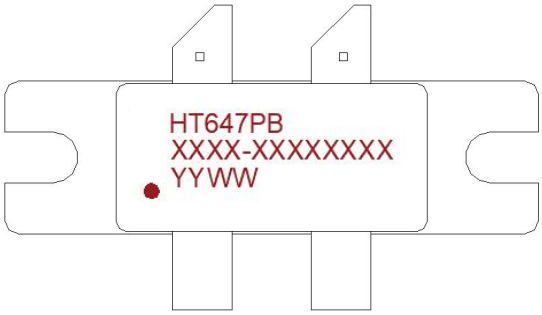


CW, Gain and Efficiency vs Pout

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 600mA test on HOTLO Application Board

Package Marking and Dimensions

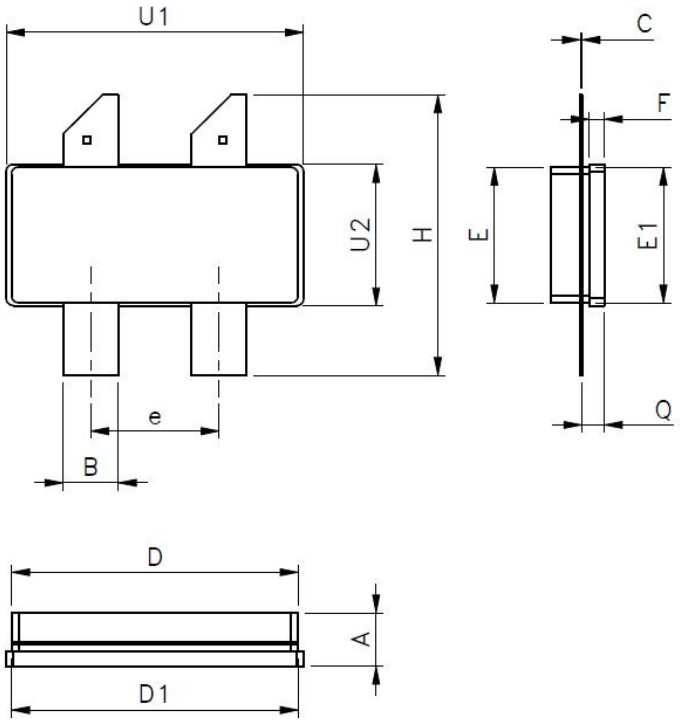




- Line1 (fixed): Device name in W/O
- Line2 (unfixed): Marking Lot No in W/O (Sample: E596-EERA0001)
- Line3 (unfixed): Date Code

This Marking SPEC only stipulates the content of Marking. For marking requirements such as font and size, please refer to the latest version of “Holto Product Printing Specification”

Marking

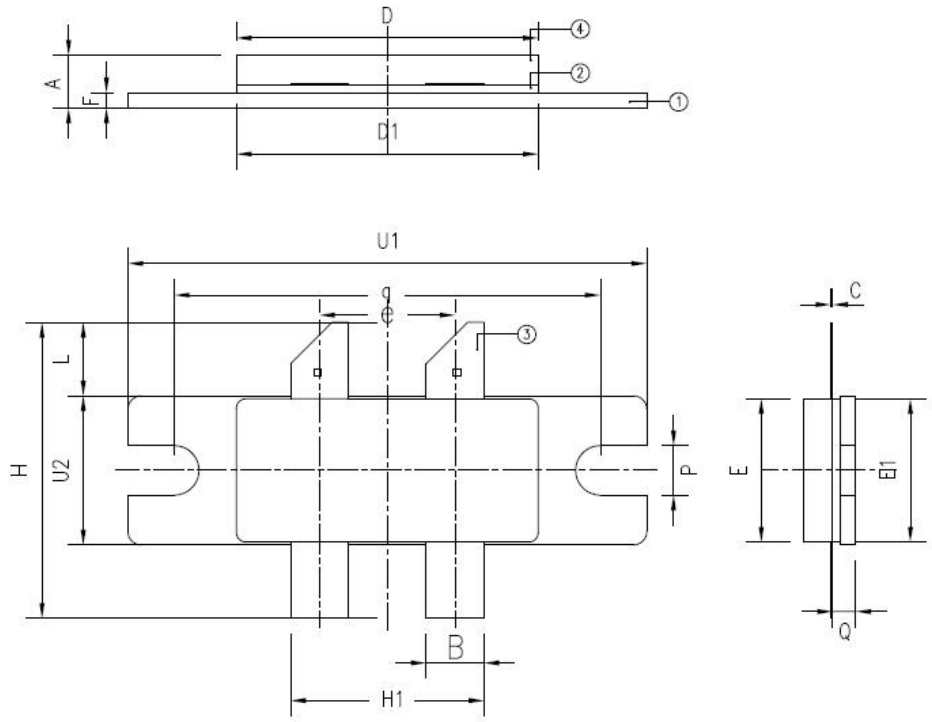


Symbol	Dimesions in Milimeters			Dimesions in Inches		
	Min.	Mon.	Max.	Min.	Mon.	Max.
A	3.12	3.69	4.26	0.123	0.145	0.168
B	3.69	3.81	3.93	0.145	0.150	0.155

C	-	0.11	-	-	0.004	-
D	19.61	19.81	20.01	0.772	0.780	0.788
D1	19.66	19.81	19.96	0.774	0.780	0.786
E	9.273	9.4	9.527	0.365	0.370	0.375
E1	9.28	9.4	9.52	0.365	0.370	0.375
F	0.95	1.02	1.09	0.037	0.040	0.043
H	19.38	19.43	19.48	0.763	0.765	0.767
Q	1.46	1.53	1.6	0.057	0.060	0.063
U1	20.51	20.58	20.65	0.807	0.810	0.813
U2	9.71	9.78	9.85	0.382	0.385	0.388
e	8.77	8.89	9.01	0.345	0.350	0.355

Package Dimensions

ACC2110S-4L Earless Flanged Ceramic Package; 4 leads



Symbol	Dimesions in Milimeters			Dimesions in Inches		
	Min.	Mon.	Max.	Min.	Mon.	Max.
A	3.55	3.71	3.86	0.140	0.146	0.152
B	3.68	3.81	3.94	0.145	0.150	0.155
C	0.04	0.11	0.18	0.002	0.004	0.007
D	19.61	19.81	20.01	0.772	0.780	0.788
D1	19.61	19.81	20.01	0.772	0.780	0.788
E	9.28	9.40	9.52	0.365	0.370	0.375

E1	9.28	9.40	9.52	0.365	0.370	0.375
F	0.95	1.02	1.09	0.037	0.040	0.043
H	18.93	19.43	19.93	0.745	0.765	0.785
H1	12.57	12.70	12.83	0.495	0.500	0.505
L	4.71	4.83	4.95	0.185	0.190	0.195
P	3.12	3.25	3.38	0.123	0.128	0.133
Q	1.43	1.53	1.63	0.056	0.060	0.064
q	-	27.94	-	-	1.10	-
U1	33.91	34.04	34.16	1.335	1.340	1.345
U2	9.71	9.78	9.85	0.382	0.385	0.388
e	-	8.89	-	-	0.35	-

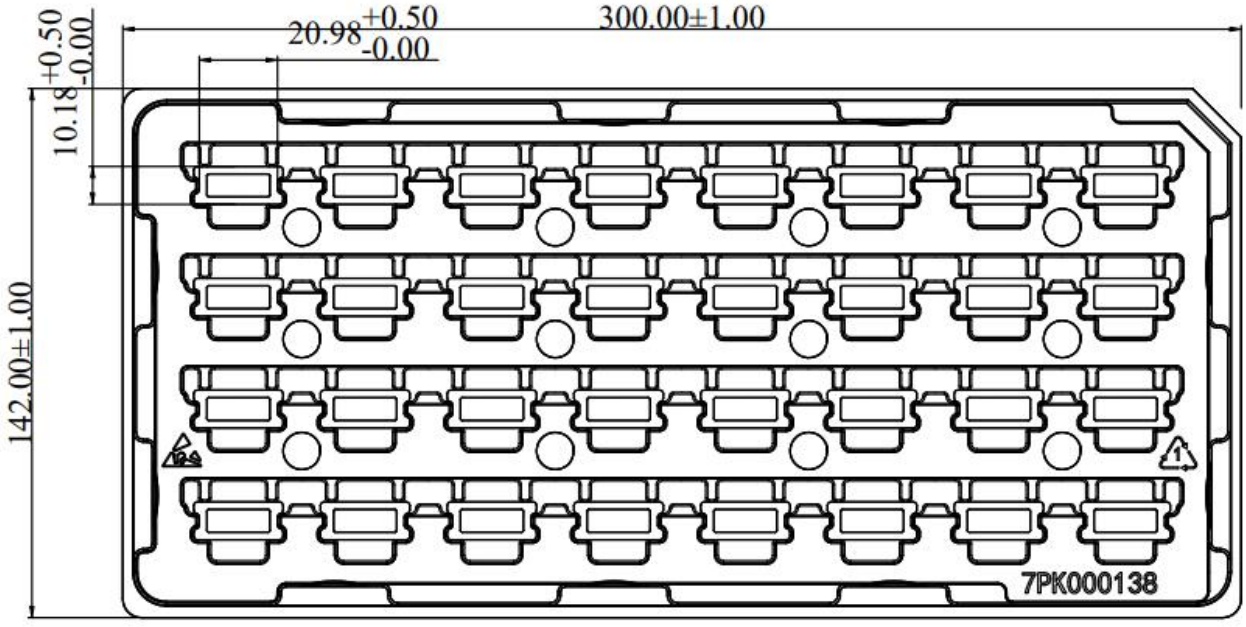
Package Dimensions

ACC2110B-4L Flanged Ceramic Package; 2 mounting holes; 4 leads

Packing Information

HT647P：

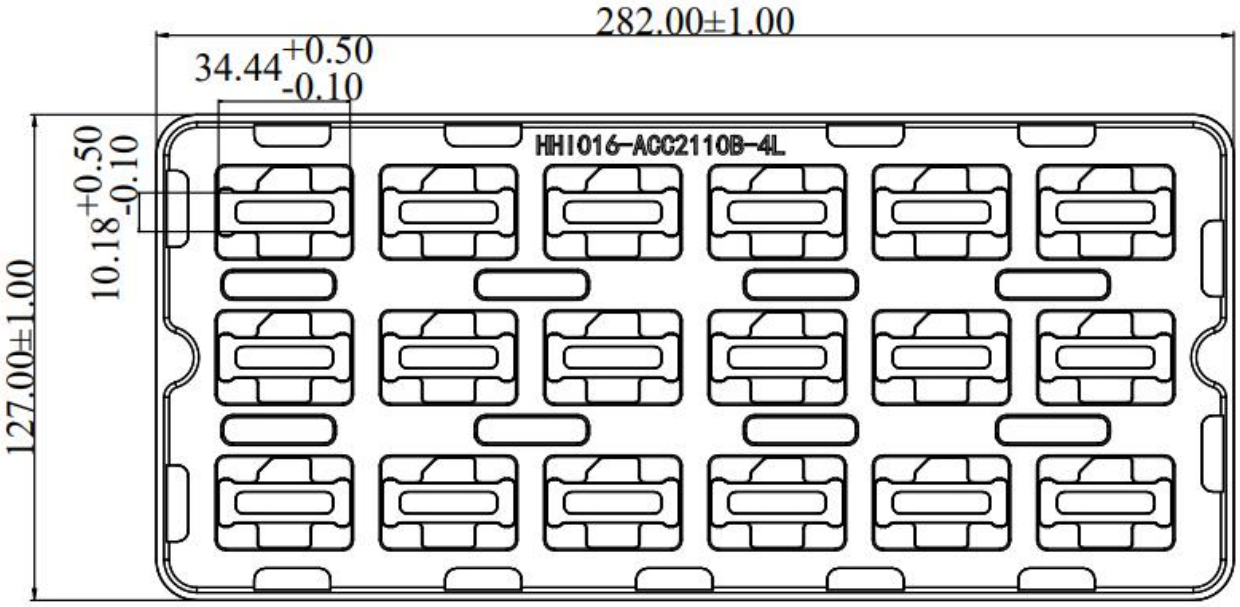
Package Type	Qty/Tray(pcs)	Qty/Box(pcs)	Qty/Carton(pcs)
ACC2110S-4L	32	160	960



Tray Packaging Descriptions

HT647PB：

Package Type	Qty/Tray(pcs)	Qty/Box(pcs)	Qty/Carton(pcs)
ACC2110B-4L	18	90	540



Tray Packaging Descriptions

Handling Precautions

Parameter	Grade
Moisture Sensitivity Level MSL	3

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	JESD22-A114
ESD – Human Body Model (MM)	Class A	EIA/JESD22-A115
ESD – Charged Device Model (CDM)	Class III	JESD22-C101

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

Datasheet Status

Document status	Product status	Definition
Objective Datasheet	Design simulation	Product objective specification
Preliminary Datasheet	Customer sample	Engineering samples and first test results
Product Datasheet	Mass production	Final product specification

Abbreviations

Acronym	Definition
LDMOS	Laterally-Diffused Metal-Oxide Semiconductor
CW	Continuous Waveform

Revision history

Document ID	Datasheet Status	Release Date	Revision Version
Rev 3.2	Product	Mar. 2023	New format based on English version datasheet
Rev 3.3	Product	Sept. 2023	Update TBD information
Rev 3.4	Product	Mar. 2024	Version released after re review
Rev 3.5	Product	Aug. 2024	Update package information

Contact Information

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