

Description

The HTH7G14S030H(B) is an unmatched discrete LDMOS Power Amplifier with 30W saturated output power covering frequency range from 1.8 - 1400 MHz.

Features

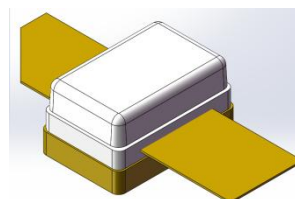
- Operating Frequency Range: 1.8 - 1400 MHz
- Operating Drain Voltage: 28-50V
- Saturation Output Power: 30W
- Excellent thermal stability due to low thermal resistance package
- Enhanced robustness design without device degradation
- Internally integrated enhanced ESD design

Applications

- Analog and Digital Broadcasting
- Meteorological and Aviation Radar
- Private network communication base station
- Industrial Laser Sources and Plasma Equipment
- Various nuclear magnetic resonance instruments
- Particle accelerator

Ordering Information

Part Number	Description
HTH7G14S030H(B)	Tray Package
HTH7G14S030H(B) EVB	1400MHz EVB

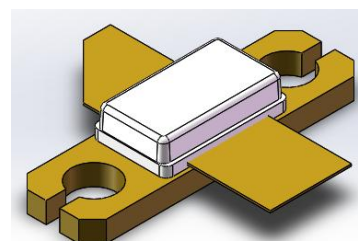


ACC0906S-2L

Earless Flanged balanced

Air Cavity Ceramic Package; 2 Leads

HTH7G14S030H



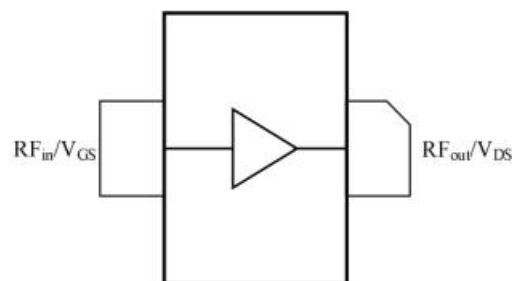
ACC0906B-2L

Flanged balanced

Air Cavity Ceramic Package; 2 Leads

2 Mounting Holes

HTH7G14S030HB



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor

Pin Connections

Typical Performance

RF Characteristics (CW)

Freq (MHz)	P1dB (dBm)	Eff (%)@P1dB	Gain (dB)	P3dB (dBm)	Eff(%)@P3dB
2	42.91	76.15	30.74	44.38	85.21
5	43.13	77.49	30.61	44.38	85.59
15	43.37	77.00	29.92	44.37	83.93
30	43.51	74.85	28.69	44.50	81.47

Test conditions unless otherwise noted: 25 °C, VDD = +48Vdc, IDQ = 160mA, Vgs=2.97V CW test on HOTLO Application Board

RF Characteristics (Pulsed CW)

Freq (MHz)	P1dB (dBm)	Eff (%)@P1dB	Gain (dB)	P3dB (dBm)	Eff(%)@P3dB
1400	44.89	59.55	17.16	45.64	62.04

Test conditions unless otherwise noted: 25 °C, VDD = +50Vdc, IDQ = 100mA PW = 100us, DC= 10% test on HOTLO Application Board

Absolute Maximum Ratings

Parameter	Range/Value	Unit
Drain voltage (V _{DSS})	-0.5 to +105	V
Gate voltage (V _{GS})	-6 to +10	V
Storage Temperature (T _{STG})	-55 to +150	°C
Junction Temperature (T _J)	+225	°C

Electrical Specification

DC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Breakdown Voltage V _{(BR)DSS}	Vgs=0V, Ids=100uA	105	-	-	V
Gate-Source Threshold Voltage V _{GS(th)}	Vgs=Vds, Ids=100uA	1.8	2.1	2.4	V
Drain Leakage Current Idss	Vgs=0V, Vds=50V	0.5	5	100	nA
Gate Leakage Current Igss	Vgs=5V, Vds=0V	0.5	3	100	nA

Load Mismatch Test

Condition	Test Result
VSWR=65:1, at all Phase Angles, V _{DD} = +50Vdc, I _{DQ_Carrier} = 100mA, CW PAVG = 30W, Frequency 1400MHz test on HOTLO Application Board	No Device Degradation

Thermal Information

Parameter	Condition	Value (Typ)	Unit
Thermal Resistance Junction to Case (R_{TH})	$V_{DD}=50V, I_{DQ}=150mA, T_{case}=25^{\circ}C, PL=30W, C$ W	3.5	$^{\circ}C / W$

Load Pull Performance Carrier

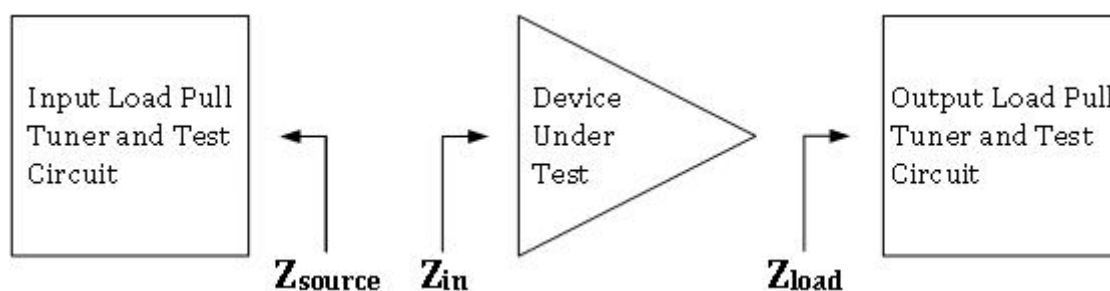
Test conditions unless otherwise noted: 25 °C, VDD = +50Vdc, IDQ= 100mA, PW = 40us, DC= 4%

Max Output Power						
Freq (MHz)	Z_source (Ω)	Z_load [1] (Ω)	Gain (dB)	P3dB (dBm)	P3dB (W)	Eff (%)
1200	1.85+2.5	7.72+6.62	19.50	46.62	45.92	64.8
1400	1.76+0.88	5.4+4.75	18.30	46.67	46.45	63.3

[1] Load impedance for optimum P3dB pout

Max Drain Efficiency						
Freq (MHz)	Z_source (Ω)	Z_load [2] (Ω)	Gain (dB)	P3dB (dBm)	P3dB (W)	Eff (%)
1200	1.85+2.5	5.9+8.65	20.52	46.15	41.21	71.03
1400	1.76+0.88	4.73+7.67	20.40	45.90	38.90	70.92

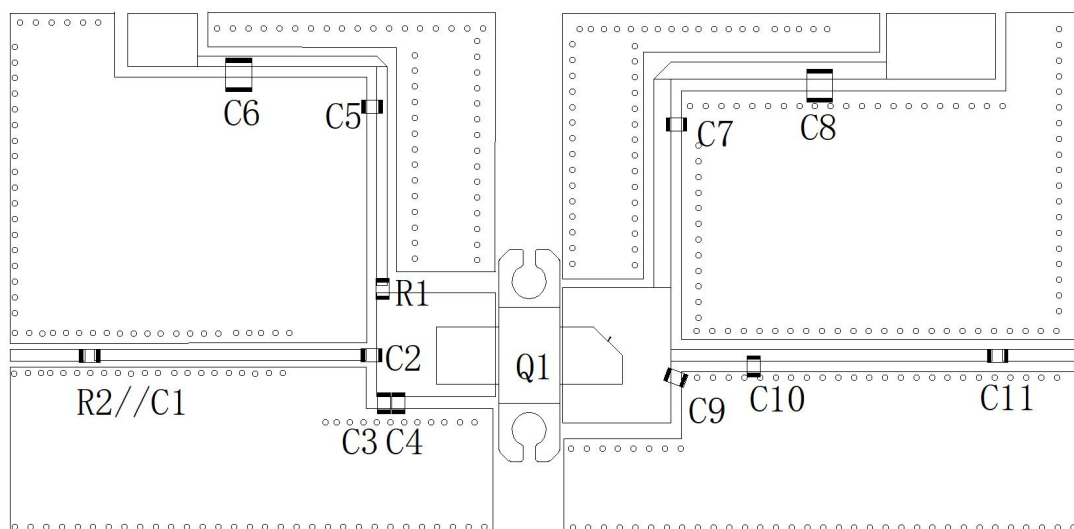
[2] Load impedance for optimum P3dB efficiency



Z_{source} : Measured impedance presented to the input of the device at the package reference plane

Z_{load} : Measured impedance presented to the output of the device at the package reference plane

HTH7G14S030H(B) 1400MHz Reference Design

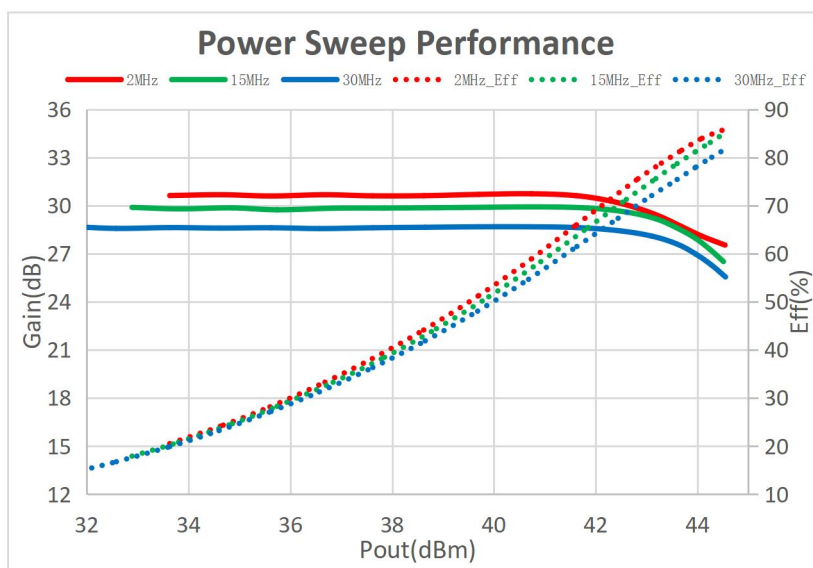


EVB Layout

Bill of Materials (BoM) - HTH7G14S030H(B) 1400MHz Reference Design

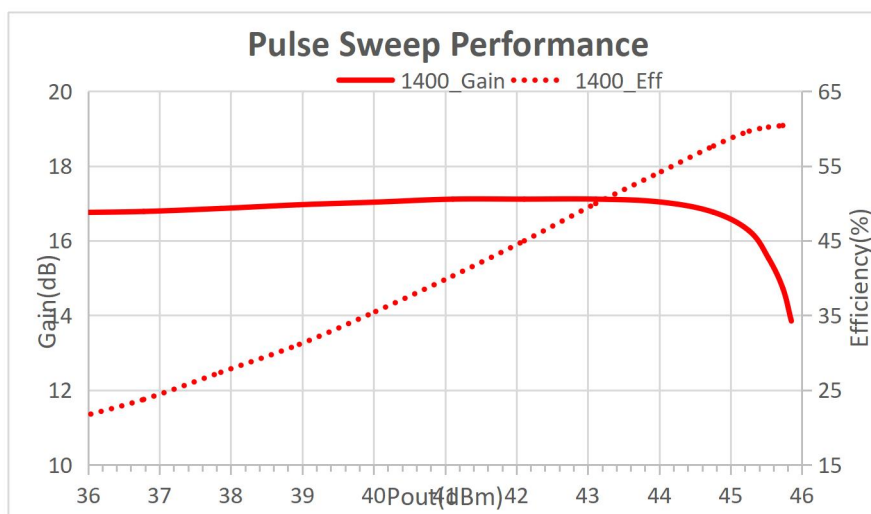
Reference	Value	Description	Manufacturer	P/N
Q1	-	30W, 1.8 - 1400 MHz LDMOS PA	Holto	HTH7G14S030H(B)
C1	16pF	0805 Chip Capacitor	Murata	GQM2195C2E160GB12D
C2\C5\C7\C11	47pF	0805 Chip Capacitor	Murata	GQM2195G2E470JB12D
C3	5.6pF	0805 Chip Capacitor	Murata	GQM2195C2E5R6BB12D
C4	2.7pF	0805 Chip Capacitor	Murata	GQM2195C2E2R7CB12D
C9	1.5pF	0805 Chip Capacitor	Murata	GQM2195C2E1R5BB12D
C10	6.8pF	0805 Chip Capacitor	Murata	GQM2195C2E6R8CB12D
C6\C8	10uF	1210 Chip Capacitor	Murata	GRM32ER61H106KA12L
R1	7.5 Ω	0805 Chip Resistor		
R2	1.6k Ω	0805 Chip Resistor		
PCB	Rogers 4350B (er = 3.5), 20 mil, 35 μ m (1oz)			

Performance Plots



CW, Gain and Efficiency vs Pout

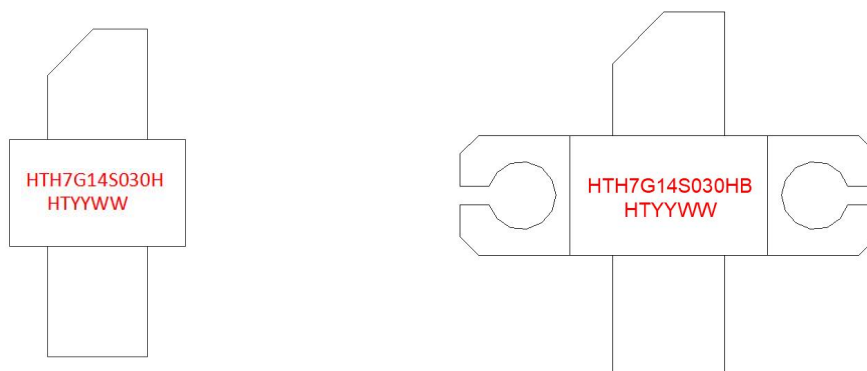
Test conditions unless otherwise noted: 25 °C, VDD = +48Vdc, IDQ = 160mA, Vgs=2.97V test on HOTLO Application Board



Pulsed CW, Gain and Efficiency vs Pout

Test conditions unless otherwise noted: 25 °C, VDD = +50Vdc, IDQ= 100mA, PW = 100us, DC= 10% test on HOTLO Application Board

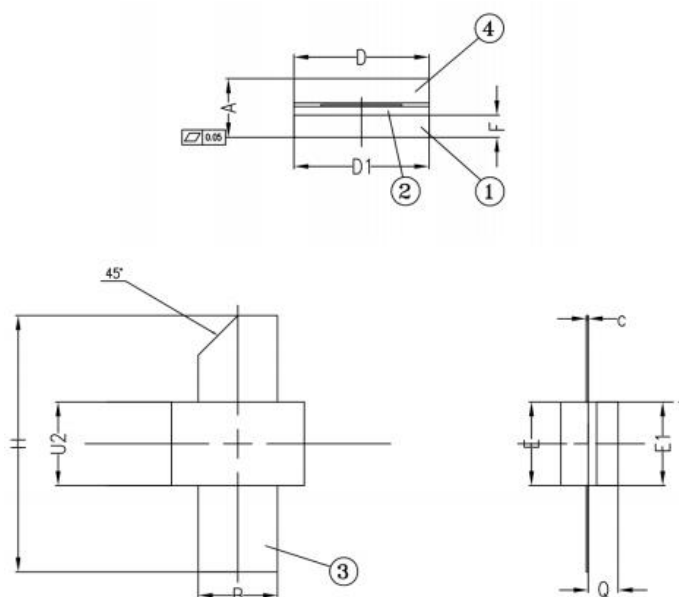
Package Marking and Dimensions



- Line1 (fixed): Device name in W/O
- Line2 (unfixed): HT+Date Code

This Marking SPEC only stipulates the content of Marking. For marking requirements such as font and size, please refer to the latest version of "Holto Product Printing Specification"

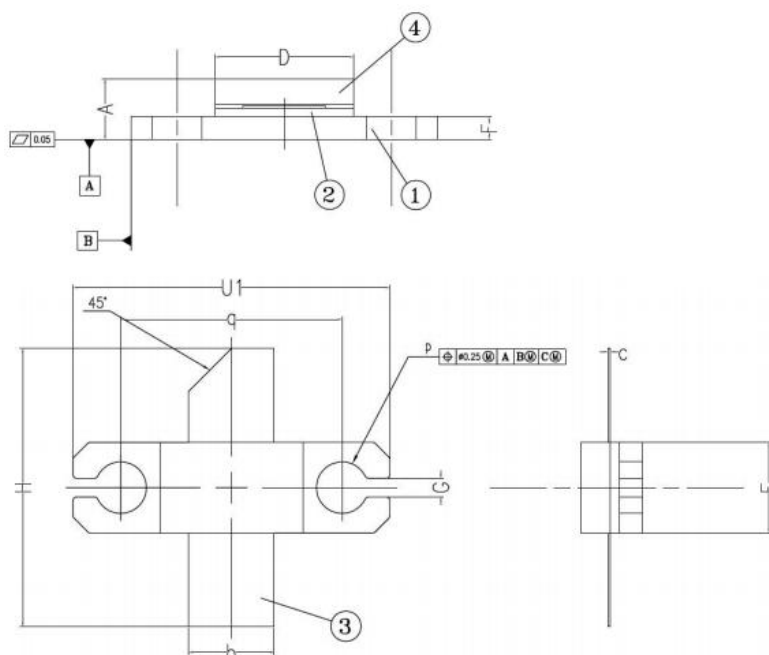
Marking



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Mon.	Max.	Min.	Mon.	Max.
A	3.84	3.98	4.12	0.151	0.157	0.162
B	5.37	5.50	5.63	5.211	0.217	0.222
C	0.11	0.13	0.15	0.004	0.005	0.006
D	9.07	9.20	9.33	0.357	0.362	0.367
D1	9.07	9.20	9.33	0.357	0.362	0.367
E	5.67	5.80	5.93	0.223	0.228	0.233
E1	5.67	5.80	5.93	0.223	0.228	0.233
F	1.37	1.50	1.63	0.054	0.059	0.064
H	17.30	17.80	18.30	0.681	0.701	0.720
Q	1.95	2.08	2.21	0.077	0.082	0.087
U2	5.67	5.80	5.93	0.223	0.228	0.233

Package Dimensions

ACC0906S-4L Earless Flanged Air Cavity Ceramic Package; 2 Leads



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Mon.	Max.	Min.	Mon.	Max.
A	3.84	3.98	4.12	0.151	0.157	0.162
b	5.37	5.50	5.63	5.211	0.217	0.222
c	0.11	0.13	0.15	0.004	0.005	0.006
D	9.07	9.20	9.33	0.357	0.362	0.367
E	5.67	5.80	5.93	0.223	0.228	0.233
F	1.37	1.50	1.63	0.054	0.059	0.064
G	1.07	1.20	1.33	0.042	0.047	0.052
H	17.30	17.80	18.30	0.681	0.701	0.720
p	3.05	3.3	3.55	0.120	0.130	0.140
q	14.07	14.20	14.33	0.554	0.559	0.564
U1	20.17	20.30	20.43	0.794	0.799	0.804

Package Dimensions

ACC0906B-2L Flanged balanced Air Cavity Ceramic Package; 2 Leads; 2 Mounting Holes

Tape and Reel Information


Package Type	Qty/Tray(pcs)	Qty/Box(pcs)
ACC0906B-2L	30	300



Tape & Reel Packaging Descriptions

Handling Precautions

Parameter	Grade
Moisture Sensitivity Level MSL	3

Parameter	Rating	Standard	
ESD – Human Body Model (HBM)	Class 1B	JESD22-A114	
ESD – Human Body Model (MM)	Class A	EIA/JESD22-A115	
ESD – Charged Device Model (CDM)	Class III	JESD22-C101	

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

Datasheet Status

Document status	Product status	Definition
Objective Datasheet	Design simulation	Product objective specification
Preliminary Datasheet	Customer sample	Engineering samples and first test results
Product Datasheet	Mass production	Final product specification

Abbreviations

Acronym	Definition
LDMOS	Laterally-Diffused Metal-Oxide Semiconductor
CW	Continuous Waveform

Revision history

Document ID	Datasheet Status	Release Date	Revision Version
Rev 1.4	Objective	March 2023	New format based on English version datasheet
Rev 2.0	Product	Sept. 2023	Update TBD information
Rev 2.1	Product	March 2024	Version released after re review

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations and information about HOTLO:

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For technical questions and application information:

- Email: andetech@andesource.com

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