HTH8G07P400H(B)

400W, 1.8 - 700 MHz LDMOS Amplifier

Product datasheet

Description

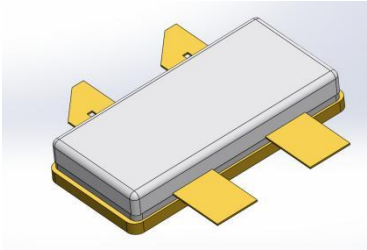
The HTH8G07P400H(B) is an unmatched discrete LDMOS Power Amplifier with 400W saturated output power covering frequency range from 1.8 - 700 MHz.

Features

- Operating Frequency Range: 1.8 - 700 MHz
- Operating Drain Voltage: +50V
- Saturation Output Power: 400W
- Internally Unmatched device
- Excellent thermal stability due to low thermal resistance package
- Enhanced robustness design without device degradation
- Internally integrated enhanced ESD design

Applications

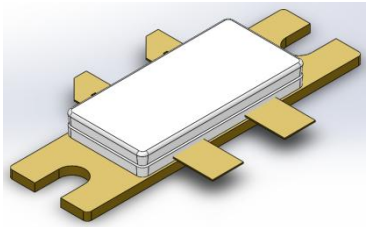
- Analog and Digital Broadcasting
- Meteorological and Aviation Radar
- Private network communication base station
- Industrial Scientific Medical (ISM)
  - Laser generation
  - Plasma generation
  - Particle accelerators
  - MRI, RF ablation and skin treatment
  - Industrial heating, welding and drying systems



ACC2110S-4L

Earless Flanged balanced
Air Cavity Ceramic Package; 4 Leads

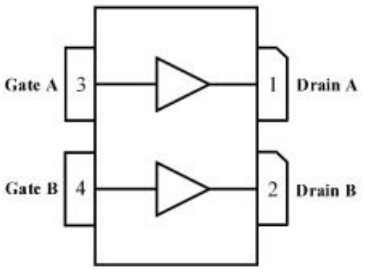
HTH8G07P400H



ACC2110B-4L

Flanged balanced
Air Cavity Ceramic Package; 4 Leads,
2 Mounting holes

HTH8G07P400HB



Note: Exposed backside of the package is the source terminal for the transistor

Pin Connections

Ordering Information

Part Number	Description
HTH8G07P400H(B)	Tray Package
HTH8G07P400H(B)EVB	470 -700 MHz EVB

Typical Performance

RF Characteristics (Pulsed-CW)

Freq (MHz)	Gain(dB)	P1dB (dBm)	Eff(%) @P1dB	P3dB (dBm)	Eff(%) @P3dB
470	19.52	55.65	42.29	56.31	42.10
500	20.44	55.95	43.90	56.70	45.87
550	20.81	54.20	35.63	56.12	42.88
600	23.26	56.10	51.78	57.17	56.14
650	21.95	56.10	58.64	56.97	62.48
700	19.80	55.71	55.65	56.52	58.09

Test conditions unless otherwise noted: 25 °C, VDD = +48Vdc, IDQ =400mA, PW = 100us, DC= 10% test on HOTLO Application Board

RF Characteristics (Pulsed-CW)

Freq (MHz)	Gain(dB)	P5dB (dBm)	Eff(%) @P5dB	PBO Gain (48.5 dBm)	PBO Eff(%) @48.5dBm
350	26.72	56.00	62.87	26.63	56.57
360	27.71	55.63	63.32	27.71	61.96
370	27.52	55.35	62.94	27.24	64.77

*Test conditions unless otherwise noted: 25 °C, VDD = +48Vdc, IDQ-carry =500mA,*Vgs-peak=1.8V，*PW = 100us, DC= 10% test on HOTLO Application Board*

Absolute Maximum Ratings

Parameter	Range/Value	Unit
Drain voltage (V_{DSS})	-0.5 to +110	V
Gate voltage (V_{GS})	-5 to +10	V
Operating Voltage (V_{DS})	0 to +50	
Storage Temperature (T_{STG})	-55 to +150	°C
Junction Temperature (T_J)	-40 to +225	°C

Electrical Specification

DC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Breakdown Voltage $V_{(BR)DSS}$	Vgs=0V, Ids=180uA	110	-	-	V
Gate-Source Threshold Voltage $V_{GS(th)}$	Vds=10V, Ids=180uA	-	2.2	-	V
Drain Leakage Current I_{DSS}	Vgs=0V, Vds=110V	-	-	10	uA
Gate Leakage Current I_{GSS}	Vgs=10V, Vds=0V	-	-	1	uA

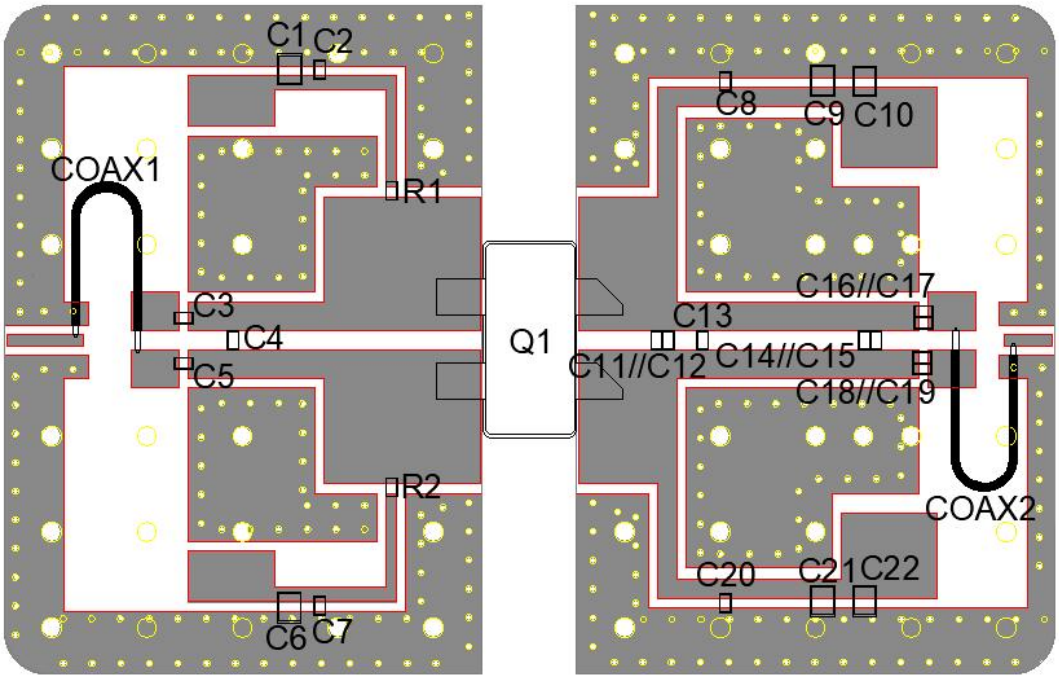
Load Mismatch Test

Condition	Test Result
VDD=48V， IDQ=500mA， Vgs-peak=1.8V， Freq=360MHz， Pavg=70W， W-CDMA VSWR 10:1	No Device Degradation

Thermal Information

Parameter	Condition	Value (Typ)	Unit
Thermal Resistance Junction to Case (R_{TH})	VDD=48V， IDQ-carry=500mA， Vgs-peak=1.8V，Tcase=25℃，Pavg=70W， LTE 20MHz	0.6	°C /W

HTH8G07P400H(B) 470 - 700 MHz Reference Design

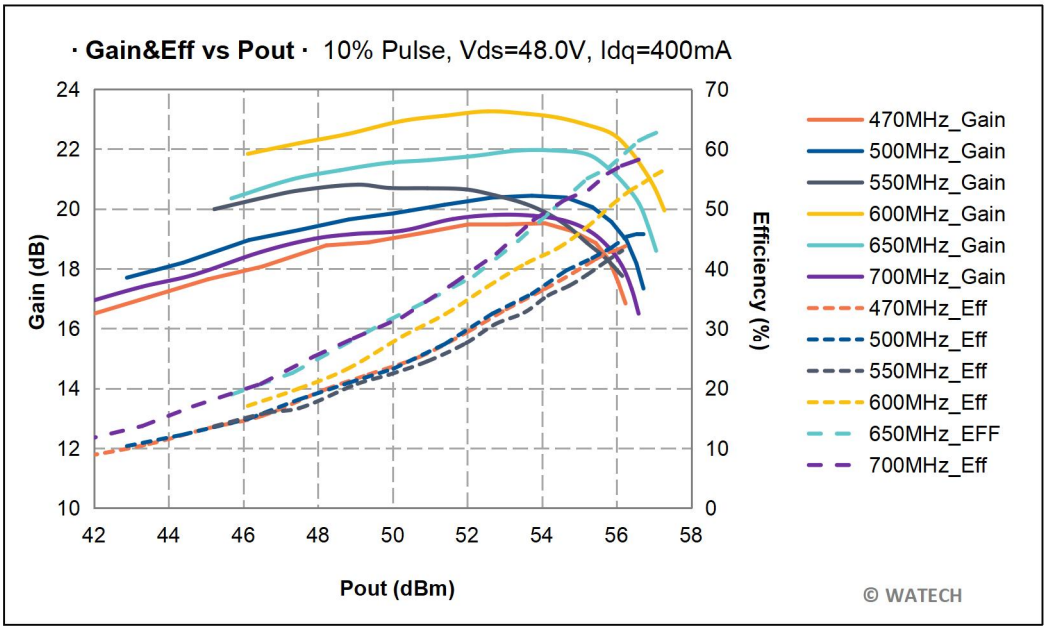


EVB Layout

Bill of Materials (BoM) - HTH8G07P400H(B) 470 - 700 MHz Reference Design

Reference	Value	Description	Manufacturer	P/N
Q1	-	400W, 1.8 - 700 MHz LDMOS PA	Holto	HTH8G07P400H(B)
C12	10pF	10pF Chip Capacitor	Murata	GQM2195C2E100JB12
C2,C3,C5,C7,C8,C16,C17,C18,C19,C20	100pF	100pF Chip Capacitors	Murata	GQM2195C2E101JB12D
C1,C6,C10,C22	4.7uF	4.7uF Chip Capacitors	Murata	GCM32DC72A475KE02L
C4	8.2pF	8.2pF Chip Capacitors	Murata	GQM2195G2E8R2BB12
C11	2.4pF	2.4pF Chip Capacitors	Murata	GQM2195G2E2R4BB12
C13	6.2pF	6.2pF Chip Capacitors	Murata	GQM2195G2E6R2BB12
C9,C21	1nF	1nF Chip Capacitors	Murata	GRM3195C2A102JA01D
C14	3.3pF	3.3pF Chip Capacitors	Murata	GQM2195G2E3R3BB12
C15	5.1pF	5.1pF Chip Capacitors	Murata	GQM2195G2E5R1BB12
COAX1,COAX2		50Ohm Coax, 120 mm	Arbitrary	Arbitrary
PCB	Rogers4350B(er=3.5),20mil,35 µm (1oz)			

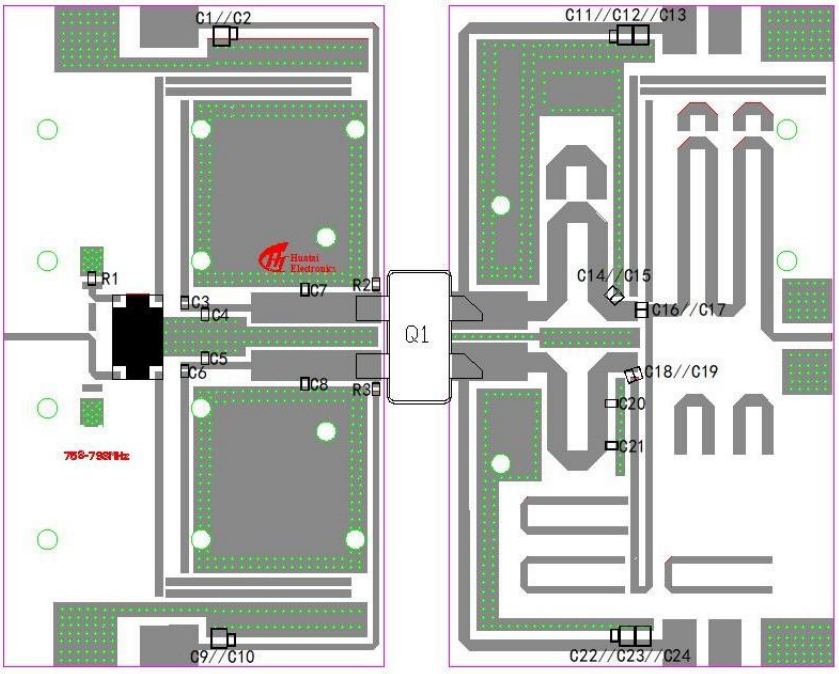
Performance Plots



Pulsed CW, Gain and Efficiency vs Pout

Test conditions unless otherwise noted: 25 °C, VDD = +48Vdc, IDQ= 400mA, PW = 100us, DC= 10% test on HOTLO Application Board

HTH8G07P400H(B) 350 - 370 MHz Reference Design

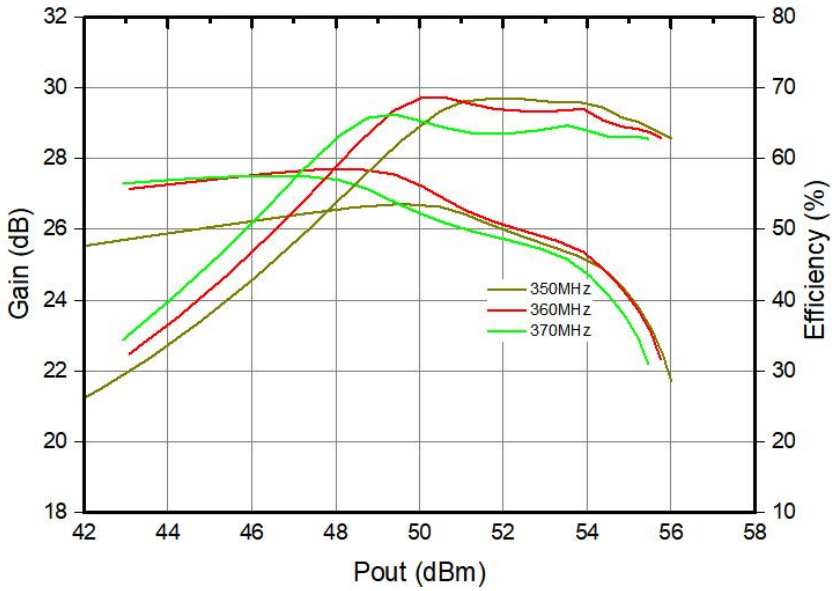


EVB Layout

Bill of Materials (BoM) - HTH8G07P400H(B) 350 - 370 MHz Reference Design

Reference	Value	Description	Manufacturer	P/N
Q1	-	400W, 1.8 - 700 MHz LDMOS PA	Holto	HTH8G07P400H(B)
R1,R2,R3	50 Ohm	50 Ohm	KOA Speer	RN732BTTD50R0B25
C1,C9,C12,C13, C23, C24	4.7uF	4.7uF Chip Capacitors	Murata	GCM32DC72A475KE02L
C2,C3,C6,C10,C11,C16,C17,C18,C19,C22	100pF	100pF Chip Capacitors	Murata	GQM2195C2E101JB12D
C4,C5	36pF	36pF Chip Capacitors	Murata	GQM2195C2E360JB12
C7,C8	43pF	43pF Chip Capacitors	Murata	GQM2195C2E430JB12
C14,C20	24pF	24pF Chip Capacitors	Murata	GQM2195C2E240JB12
C15	20pF	20pF Chip Capacitors	Murata	GQM2195C2E200JB12
C21	11pF	11pF Chip Capacitors	Murata	GQM2195C2E110JB12
PCB	Rogers4350B(er=3.5),20mil,35 µm (1oz)			

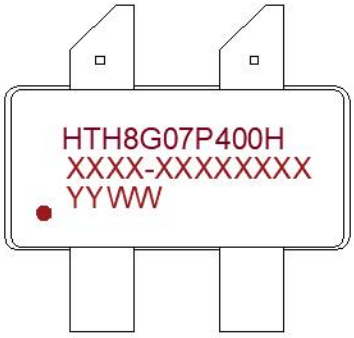
Performance Plots

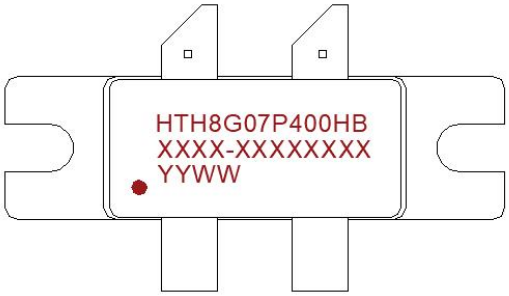


Pulsed CW, Gain and Efficiency vs Pout

*Test conditions unless otherwise noted: 25 °C, VDD = +48Vdc, IDQ-carry =500mA,*Vgs-peak=1.8V*, PW = 100us, DC= 10% test on HOTLO Application Board*

Package Marking and Dimensions

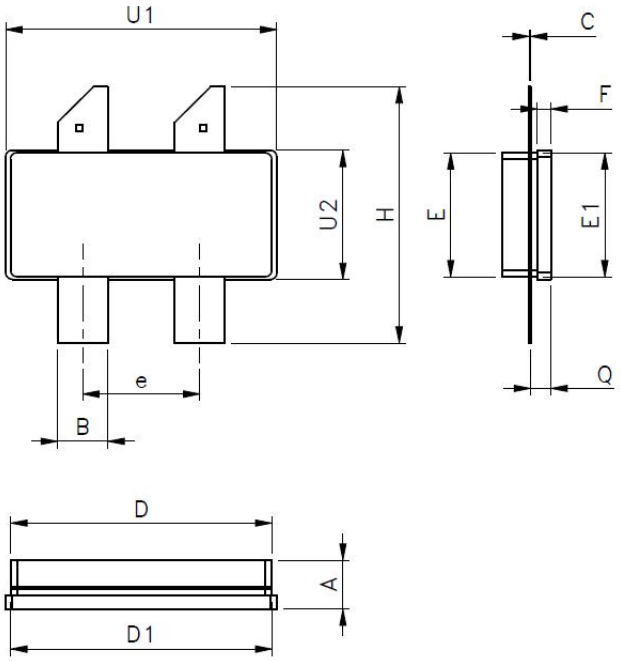




- Line1 (fixed): Device name in W/O
- Line2 (unfixed): Marking Lot No in W/O (Sample: E596-EERA0001)
- Line3 (unfixed): Date Code

This Marking SPEC only stipulates the content of Marking. For marking requirements such as font and size, please refer to the latest version of “Holto Product Printing Specification”

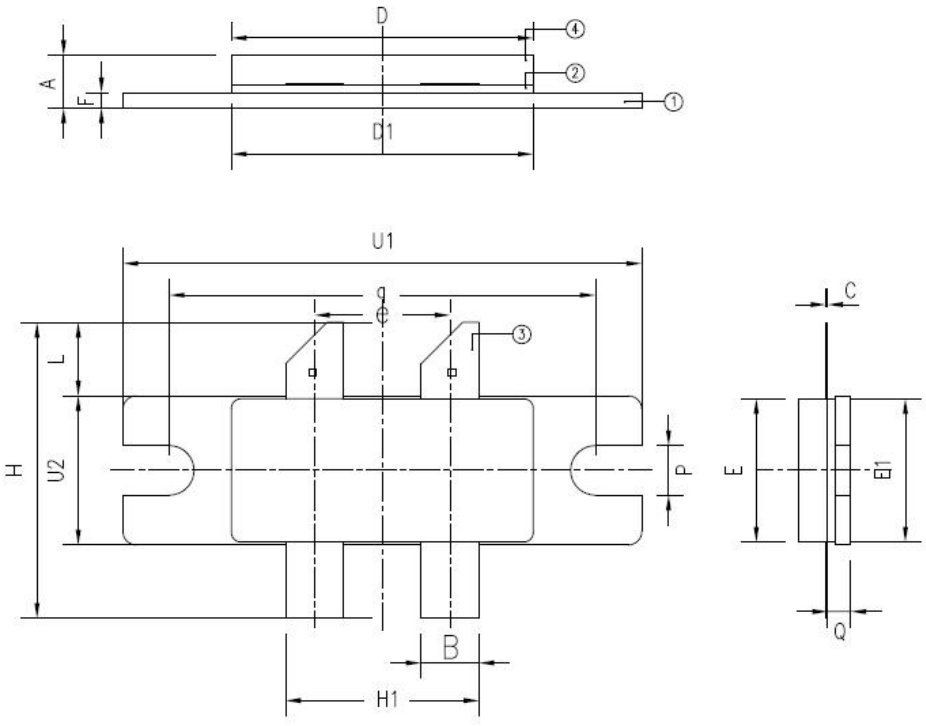
Marking



Symbol	Dimesions in Milimeters			Dimesions in Inches		
	Min.	Mon.	Max.	Min.	Mon.	Max.
A	3.12	3.69	4.26	0.123	0.145	0.168
B	3.69	3.81	3.93	0.145	0.150	0.155
C	-	0.11	-	-	0.004	-
D	19.61	19.81	20.01	0.772	0.780	0.788
D1	19.66	19.81	19.96	0.774	0.780	0.786
E	9.273	9.4	9.527	0.365	0.370	0.375
E1	9.28	9.4	9.52	0.365	0.370	0.375
F	0.95	1.02	1.09	0.037	0.040	0.043
H	19.38	19.43	19.48	0.763	0.765	0.767
Q	1.46	1.53	1.6	0.057	0.060	0.063
U1	20.51	20.58	20.65	0.807	0.810	0.813
U2	9.71	9.78	9.85	0.382	0.385	0.388
e	8.77	8.89	9.01	0.345	0.350	0.355

Package Dimensions

ACC2110S-4L Earless Flanged Ceramic Package; 4 leads



Symbol	Dimesions in Milimeters			Dimesions in Inches		
	Min.	Mon.	Max.	Min.	Mon.	Max.
A	3.55	3.71	3.86	0.140	0.146	0.152
B	3.68	3.81	3.94	0.145	0.150	0.155
C	0.04	0.11	0.18	0.002	0.004	0.007
D	19.61	19.81	20.01	0.772	0.780	0.788
D1	19.61	19.81	20.01	0.772	0.780	0.788
E	9.28	9.40	9.52	0.365	0.370	0.375
E1	9.28	9.40	9.52	0.365	0.370	0.375
F	0.95	1.02	1.09	0.037	0.040	0.043
H	18.93	19.43	19.93	0.745	0.765	0.785
H1	12.57	12.70	12.83	0.495	0.500	0.505
L	4.71	4.83	4.95	0.185	0.190	0.195
P	3.12	3.25	3.38	0.123	0.128	0.133
Q	1.43	1.53	1.63	0.056	0.060	0.064
q	-	27.94	-	-	1.10	-
U1	33.91	34.04	34.16	1.335	1.340	1.345
U2	9.71	9.78	9.85	0.382	0.385	0.388
e	-	8.89	-	-	0.35	-

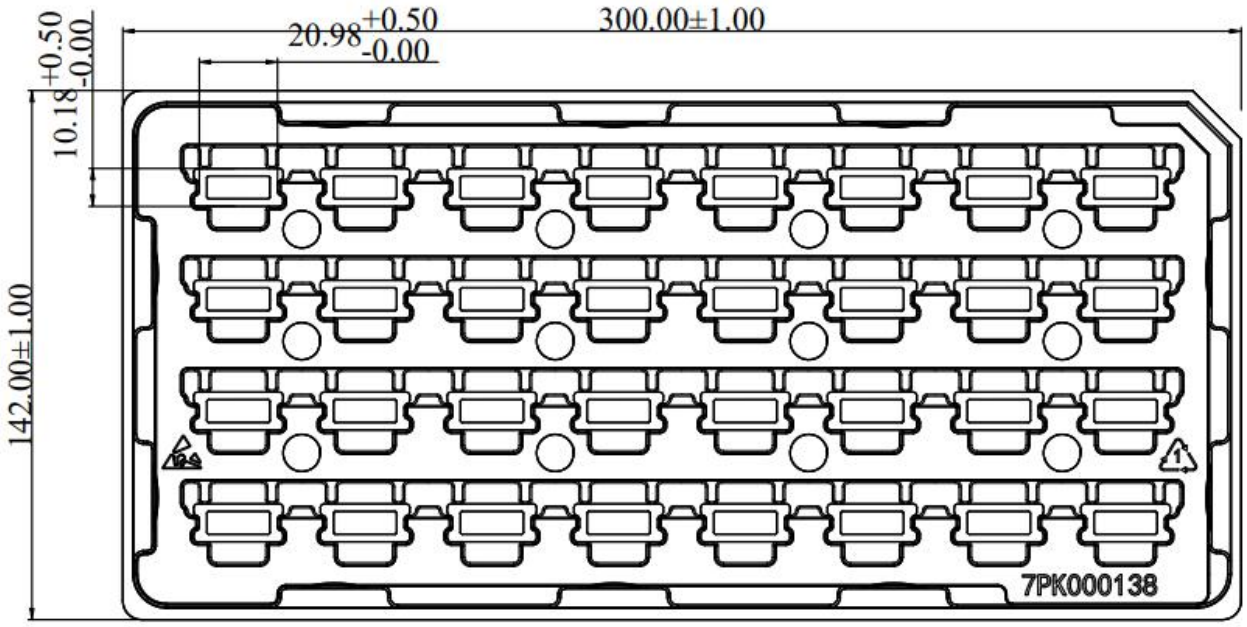
Package Dimensions

ACC2110B-4L Flanged Ceramic Package; 2 mounting holes; 4 leads

Packing Information

HTH8G07P400H：

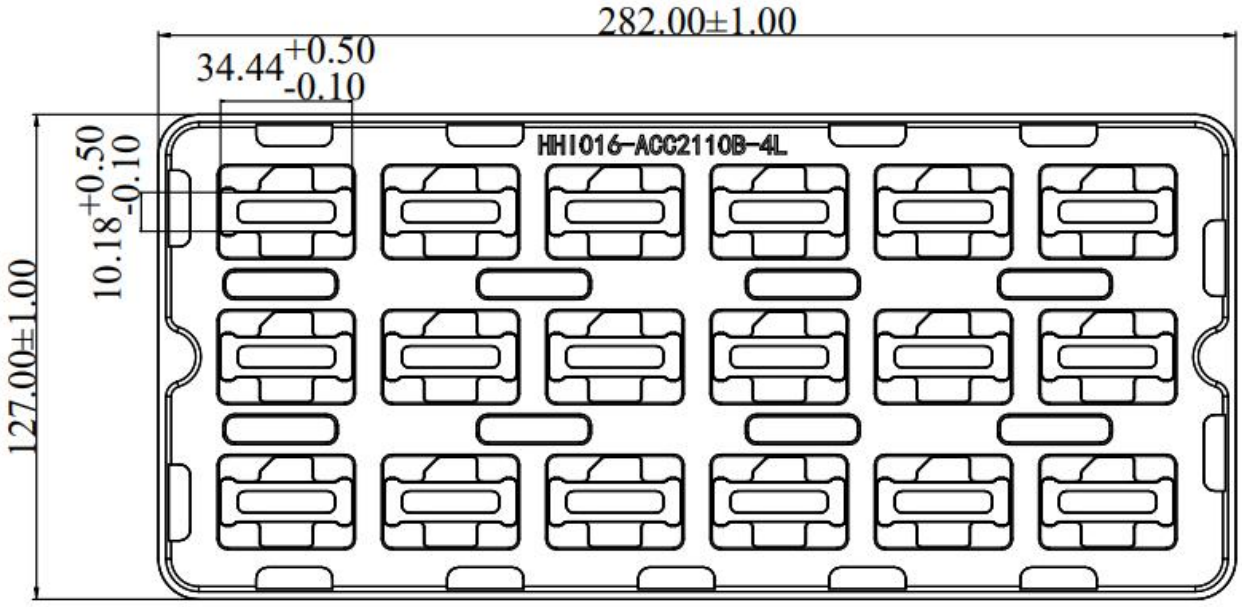
Package Type	Qty/Tray(pcs)	Qty/Box(pcs)	Qty/Carton(pcs)
ACC2110S-4L	32	160	960



Tray Packaging Descriptions

HTH8G07P400HB：

Package Type	Qty/Tray(pcs)	Qty/Box(pcs)	Qty/Carton(pcs)
ACC2110B-4L	18	90	540



Tray Packaging Descriptions

Handling Precautions

Parameter	Grade
Moisture Sensitivity Level MSL	3

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	JESD22-A114
ESD – Human Body Model (MM)	Class A	EIA/JESD22-A115
ESD – Charged Device Model (CDM)	Class III	JESD22-C101

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

Datasheet Status

Document status	Product status	Definition
Objective Datasheet	Design simulation	Product objective specification
Preliminary Datasheet	Customer sample	Engineering samples and first test results
Product Datasheet	Mass production	Final product specification

Abbreviations

Acronym	Definition
LDMOS	Laterally-Diffused Metal-Oxide Semiconductor
CW	Continuous Waveform

Revision history

Document ID	Datasheet Status	Release Date	Revision Version
Rev 1.0	Preliminary	Dec. 2021	Preliminary
Rev 1.1	Objective	March 2023	New format based on English version datasheet
Rev 2.0	Product	Sept.2023	Update TBD information
Rev 2.1	Product	Dece.2023	Update frequency information
Rev 2.2	Product	March 2024	Version released after re review
Rev 2.3	Product	June 2024	Update EVB layout design
Rev 2.4	Product	August 2024	Update package information

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations and information about HOTLO:

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