ORTUSTECH

Technical Specification

Model No. COM32T3M34ILX

(FR = 60Hz version)

3.2" (480 x 800) TFT Module

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ORTUS TECHNOLOGY CO.,LTD.

ORTUS TECHNOLOGY CONFIDENTIAL

Version 0.1 English (FR=60Hz)

This specification sheet is tentative.
This specification sheet is subject to change without notice.

History of Revision

Revision	Contents	Page	date	
Rev 0.0	First issue		2009/12/8	
Rev 0.1	Change "Set gamma curve related setting"	20	2010/1/19	

1. Summary

This documentation is for a LCD monitor model No. Dx3M34 , which has high picture quality, 16,777,216-color, 3.2" TFT display with 480 x RGB(H) x 800(V) dots .

Characteristics

16,777,216-color display (8-bit for R , G and B)
System Interface (Register setteing)
Serial Peripheral Interface (SPI)
RGB interface with 24-bit data bus (VSYNC, HSYNC, ENABLE, DOTCLK, D23-0)
Internal booster for various voltage levels to drive LC

2. General Specifications

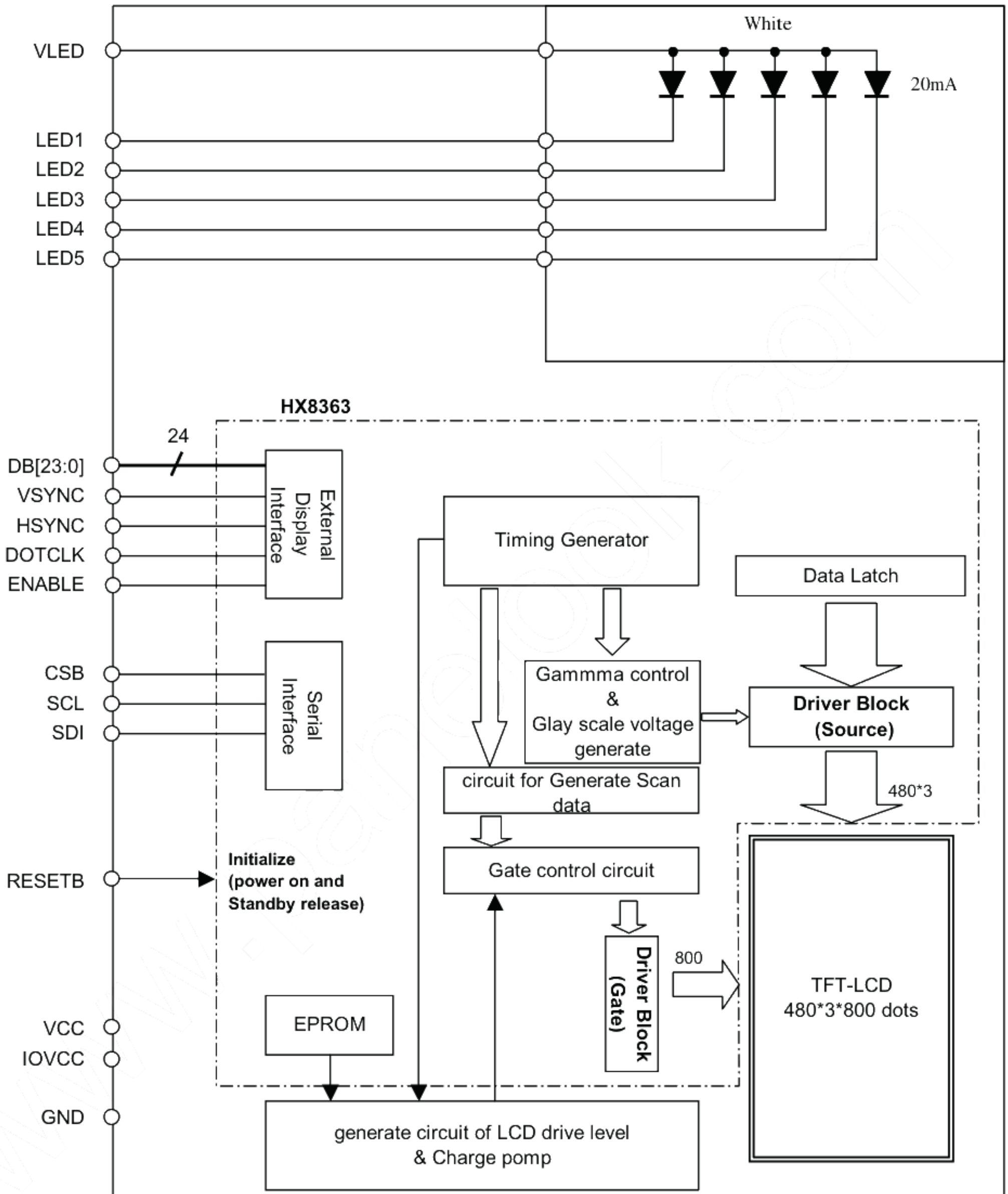
2.1 Overall specification

Item	Details	Remark
Product description	LCD monitor with internal CPU interface circuit	
Input Signal	Register : Serial Peripheral Interface (SPI) Data : 24 bit RGB interface	
Back light type	High brightness LED, side light	
Outer dimension	**.*mm(V) x **.*mm(H) x *.*mm(D)	
Weight	**.*g	
Storage temperature	-30C ~ +80C	
Operating temperature	-20C ~ +70C	Panel surface temperature

2.2 TFT Specifications

Display size		3.2 inch diagonal	
Module			
	Display type	transmissive, normally Black	
	Resolution	480 x RGB(H) x 800 (V)	
	Dot pitch	** μm(H) x *** μm(V)	
	Pixel arrangement	RGB stripe arrangement	
	Active area	**.** mm(V) x **.** mm(H)	

3. Block Diagram



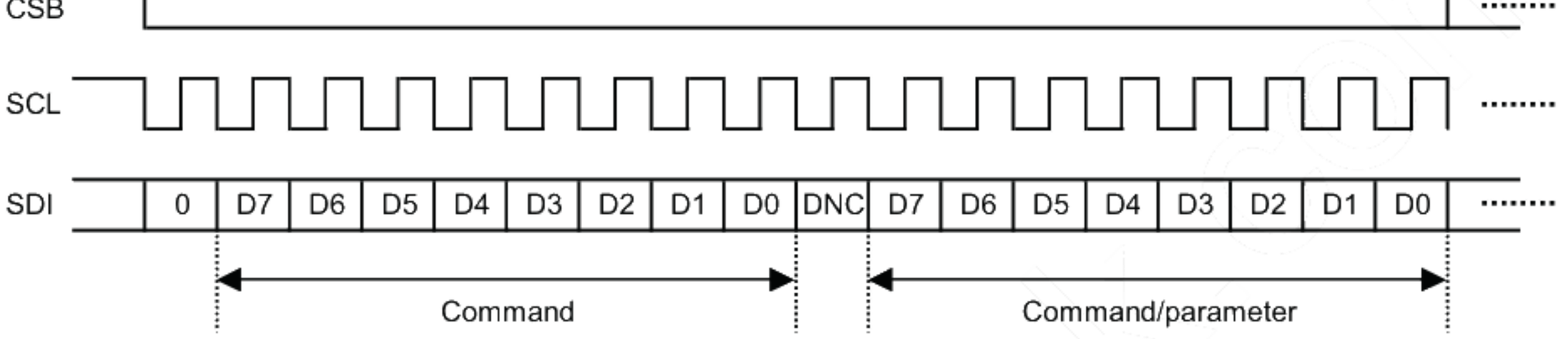
4. FPC Terminals

No.	Symbol	Details	Remark	IO
1	LED5	Backlight LED Cathode5		P
2	LED4	Backlight LED Cathode4		P
3	LED3	Backlight LED Cathode3		P
4	LED2	Backlight LED Cathode2		P
5	LED1	Backlight LED Cathode1		P
6	VLED	Power supply for Backlignt LED		P
7	VLED	Power supply for Backlignt LED		P
8	DB7	B_Data	MSB	I
9	DB6			I
10	DB5			I
11	DB4			I
12	DB3			I
13	DB2			I
14	DB1			I
15	DB0		LSB	I
16	GND	GROUND		P
17	DB15	G_Data	MSB	I
18	DB14			I
19	DB13			I
20	DB12			I
21	DB11			I
22	DB10			I
23	DB9			I
24	DB8		LSB	I
25	GND	GROUND		P
26	DB23	R_Data	MSB	I
27	DB22			I
28	DB21			I
29	DB20			I
30	DB19			I
31	DB18			I
32	DB17			I
33	DB16		LSB	I
34	GND	GROUND		P
35	HSYNC	HSYNC		I
36	VSYNC	VSYNC		I
37	RESETB	LCD Reset	L:Initialize Power_ON Reset is Required when Turning on the Power	I
38	DOTCLK	DOTCLK		I
39	CSB	3-Wire SPI Chip Select		I
40	SCL	3-Wire SPI clock		I
41	SDI	3-Wire SPI DATA input		I
42	ENABLE	ENABLE		I
43	IOVCC	Power		P
44	VCC	Power		P
45	VCC	Power		P
46	GND	GROUND		P

5. Serial Data Transfer Interface

Instructions are transferred using 3 wire serial data transfer interface. The 3 wire serial bus uses chip select line (NCS), serial input data (SDI) and serial transfer clock line (SCL).

The 3 wire serial data packet is consists of control bit DNC and transmission byte. If the control bit is low, the transmission byte is command byte. If the control bit is high, the transmission byte is stored to command register. DNC should be transferred first , followed by MSB of transmission byte.
The serial interface is initialized when NCS is high, and the falling edge of NCS enables the serial interface.



6.Instruction list

(1)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0
00	NOP	0	0	0	0	0	0	0	0	0
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
01	SWRESET	0	0	0	0	0	0	0	0	1
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
06	RDRED	0	0	0	0	0	0	1	1	0
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
07	RDGREEN	0	0	0	0	0	0	1	1	1
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
08	RDBLUE	0	0	0	0	0	1	0	0	0
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
0A	RDDPM	0	0	0	0	0	1	0	1	0
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
0B	RDDMADCTL	0	0	0	0	0	1	0	1	1
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
0C	RDDCOLMOD	0	0	0	0	0	1	1	0	0
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
0D	RDDIM	0	0	0	0	0	1	1	0	1
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
0E	RDDSM	0	0	0	0	0	1	1	1	0
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
0F	RDDSDR	0	0	0	0	0	1	1	1	1
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
10	SLPIN	0	0	0	0	1	0	0	0	0
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
11	SLPOUT	0	0	0	0	1	0	0	0	1
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
20	INVOFF	0	0	0	1	0	0	0	0	0
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
21	INVON	0	0	0	1	0	0	0	0	1
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
26	GAMSET	0	0	0	1	0	0	1	1	0
		1	GC[7:0]							
	initial	-	0	0	0	0	0	0	0	1
	recommend	-	-	-	-	-	-	-	-	-
28	DISPOFF	0	0	0	1	0	1	0	0	0
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
29	DISPON	0	0	0	1	0	1	0	0	1
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-

(2)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0
36	MADCTL	0	0	0	1	1	0	1	1	0
		1	-	-	-	-	BGR	-	SS	GS
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	0	0	0	0	0	0	0
3A	COLMOD	0	0	0	1	1	1	0	1	0
		1	-	CSEL_RGB[2:0]			-	-	-	-
	initial	-	0	1	1	1	0	0	0	0
	recommend	-	0	1	1	1	0	0	0	0
B1	SETPOWER	0	1	0	1	1	0	0	0	1
		1	-	VSN_EN	VSP_EN	VGL_EN	VGH_EN	-	VDDN_HZ	SLP
	initial	-	1	0	0	0	0	0	0	1
	recommend	-	0	1	1	1	1	0	0	0
		1	-	FS12	FS11	FS10	-	AP2	AP1	AP0
	initial	-	0	0	1	1	0	0	0	0
	recommend	-	0	0	0	0	0	0	0	1
		1	-	-	-	-	BT3	BT2	BT1	BT0
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	0	0	0	0	1	0	0
		1	DT1	DT0	DC1	DC0	DC_DIV3	DC_DIV2	DC_DVI1	DC_DVI0
	initial	-	0	0	1	1	0	0	0	0
	recommend	-	0	0	0	0	0	0	0	0
		1	-	DTPS2	DTPS1	DTPS0	-	DTP2	DTP1	DTP0
	initial	-	0	0	0	0	0	1	0	0
	recommend	-	0	0	0	0	0	0	0	0
		1	-	DTNS2	DTNS1	DTNS0	-	DTN2	DTN1	DTN0
	initial	-	0	0	0	1	0	1	1	0
	recommend	-	0	0	0	0	0	0	0	0
		1	-	-	-	BTP4	BTP3	BTP2	BTP1	BTP0
	initial	-	0	0	0	0	1	1	1	0
	recommend	-	0	0	0	1	0	0	0	0
		1	-	-	-	BTN4	BTN3	BTN2	BTN1	BTN0
	initial	-	0	0	0	0	1	1	1	0
	recommend	-	0	0	0	1	0	0	0	0
		1	VRHP7	VRHP6	VRHP5	VRHP4	VRHP3	VRHP2	VRHP1	VRHP0
	initial	-	0	0	1	0	0	1	0	0
	recommend	-	0	0	1	1	0	1	0	0
		1	VRHN7	VRHN6	VRHN5	VRHN4	VRHN3	VRHN2	VRHN1	VRHN0
	initial	-	0	0	1	0	1	1	0	0
	recommend	-	0	0	1	1	1	1	0	0
		1	-	-	VRMP5	VRMP4	VRMP3	VRMP2	VRMP1	VRMP0
	initial	-	0	0	0	1	1	0	0	1
	recommend	-	0	0	1	1	1	1	1	1
		1	-	-	VRMN5	VRMN4	VRMN3	VRMN2	VRMN1	VRMN0
	initial	-	0	0	0	1	1	0	0	1
	recommend	-	0	0	1	1	1	1	1	1
B3	SETRGBIF	0	1	0	1	1	0	0	1	1
		1	-	-	-	-	DPL	HSPL	VSPL	EPL
	initial	-	0	0	0	0	0	0	0	1
	recommend	-	0	0	0	0	0	0	0	0

(3)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0
B4	SETRGBIF	0	1	0	1	1	0	1	0	0
		1	-	-	-	-	NW[1:0]		-	-
	initial	-	0	0	0	0	1	0	0	0
	recommend	-	0	0	0	0	1	0	0	0
		1	SON[7:0]							
	initial	-	0	0	0	1	0	0	1	0
	recommend	-	0	0	0	0	1	0	0	0
		1	SOFF[7:0]							
	initial	-	0	1	1	1	0	0	1	0
	recommend	-	0	1	1	0	1	1	1	0
		1	EQS[7:0]							
	initial	-	0	0	0	1	0	0	1	0
	recommend	-	0	0	0	0	0	1	1	1
		1	EQON[7:0]							
	initial	-	0	0	0	0	0	1	1	0
	recommend	-	0	0	0	0	0	0	0	1
		1	GDON[7:0]							
	initial	-	0	0	0	0	0	0	1	1
	recommend	-	0	0	0	0	0	0	0	1
		1	GDOFF[7:0]							
	initial	-	0	1	1	0	0	0	0	0
	recommend	-	0	1	1	0	1	0	0	1
		1	GVSSP1[7:0]							
	initial	-	0	0	0	0	0	0	1	1
	recommend	-	0	0	0	0	0	0	0	1
		1	GVSSP2[7:0]							
	initial	-	0	1	0	1	1	0	1	0
	recommend	-	0	1	1	0	1	0	0	1
B9	SETRGBIF	0	1	0	1	1	1	0	0	1
		1	EXTC1[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	1	1	1	1	1	1	1
		1	EXTC2[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	0	0	0	0	0	1	1
		1	EXTC3[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	1	1	0	0	0	1	1
C1	SETDGCLUT	0	1	1	0	0	0	0	0	1
		1	-	-	-	-	-	-	-	DGC_EN
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	0	0	0	0	0	0	1
		1	D1[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	1	1	0	1	1	1	1
		1	D2[7:0]							
	initial	-	0	0	0	0	1	0	0	0
	recommend	-	1	1	0	1	0	1	1	1
		1	D3[7:0]							
	initial	-	0	0	0	1	0	0	0	0
	recommend	-	1	0	1	1	1	1	0	1
		1	D4[7:0]							
	initial	-	0	0	0	1	1	0	0	0
	recommend	-	1	0	0	1	1	0	1	0

(4)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0
C1	SETDGCLUT	1	D5[7:0]							
	initial	-	0	0	1	0	0	0	0	0
	recommend	-	0	1	1	1	1	0	1	0
		1	D6[7:0]							
	initial	-	0	0	1	0	1	0	0	0
	recommend	-	0	1	0	1	1	0	1	1
		1	D7[7:0]							
	initial	-	0	0	1	1	0	0	0	0
	recommend	-	0	0	1	1	1	1	0	1
		1	D8[7:0]							
	initial	-	0	0	1	1	1	0	0	0
	recommend	-	0	0	1	0	0	1	0	1
		1	D9[7:0]							
	initial	-	0	1	0	0	0	0	0	0
	recommend	-	0	0	0	0	1	0	0	1
		1	D10[7:0]							
	initial	-	0	1	0	0	1	0	0	0
	recommend	-	1	1	1	0	1	1	0	0
		1	D11[7:0]							
	initial	-	0	1	0	1	0	0	0	0
	recommend	-	1	1	0	1	0	0	1	0
		1	D12[7:0]							
	initial	-	0	1	0	1	1	0	0	0
	recommend	-	1	0	1	1	0	1	0	0
		1	D13[7:0]							
	initial	-	0	1	1	0	0	0	0	0
	recommend	-	1	0	0	1	1	0	1	0
		1	D14[7:0]							
	initial	-	0	1	1	0	1	0	0	0
	recommend	-	0	1	1	1	1	1	1	1
		1	D15[7:0]							
	initial	-	0	1	1	1	0	0	0	0
	recommend	-	0	1	1	0	0	1	0	1
		1	D16[7:0]							
	initial	-	0	1	1	1	1	0	0	0
	recommend	-	0	1	0	0	1	0	0	0
		1	D17[7:0]							
	initial	-	1	0	0	0	0	0	0	0
	recommend	-	0	0	1	0	1	1	0	1
		1	D18[7:0]							
	initial	-	1	0	0	0	1	0	0	0
	recommend	-	0	0	0	1	0	1	0	0
		1	D19[7:0]							
	initial	-	1	0	0	1	0	0	0	0
	recommend	-	1	1	1	1	0	1	1	0
		1	D20[7:0]							
	initial	-	1	0	0	1	1	0	0	0
	recommend	-	1	1	0	1	1	1	0	0
		1	D21[7:0]							
	initial	-	1	0	1	0	0	0	0	0
	recommend	-	1	1	0	0	0	0	0	1
		1	D22[7:0]							
	initial	-	1	0	1	0	1	0	0	0
	recommend	-	1	0	1	0	1	0	0	0

SETDGCLUT continues to the next page.

(5)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0
C1	SETDGCLUT	1	D23[7:0]							
	initial	-	1	0	1	1	0	0	0	0
	recommend	-	1	0	0	0	1	1	0	0
		1	D24[7:0]							
	initial	-	1	0	1	1	1	0	0	0
	recommend	-	0	1	0	1	1	0	0	1
		1	D25[7:0]							
	initial	-	1	1	0	0	0	0	0	0
	recommend	-	0	0	1	1	0	1	1	0
		1	D26[7:0]							
	initial	-	1	1	0	0	1	0	0	0
	recommend	-	0	0	0	1	0	1	0	1
		1	D27[7:0]							
	initial	-	1	1	0	1	0	0	0	0
	recommend	-	1	1	1	1	0	0	1	1
		1	D28[7:0]							
	initial	-	1	1	0	1	1	0	0	0
	recommend	-	1	1	0	1	0	0	1	0
		1	D29[7:0]							
	initial	-	1	1	1	0	0	0	0	0
	recommend	-	1	0	1	1	1	0	1	1
		1	D30[7:0]							
	initial	-	1	1	1	0	1	0	0	0
	recommend	-	1	0	0	0	1	1	1	0
		1	D31[7:0]							
	initial	-	1	1	1	1	0	0	0	0
	recommend	-	0	0	0	0	1	1	1	1
		1	D32[7:0]							
	initial	-	1	1	1	1	1	0	0	0
	recommend	-	0	0	0	0	1	0	0	1
		1	D33[7:0]							
	initial	-	1	1	1	1	1	1	1	1
	recommend	-	0	0	0	0	0	0	0	0
		1	D34[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	1	1	1	1	1	1	1
		1	D35[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	1	1	1	1	1	1	1
		1	D36[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	1	1	0	1	0	1	0
		1	D37[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	0	1	0	1	0	1	0
		1	D38[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	0	1	0	0	1	0	1
		1	D39[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	1	0	1	0	1	0	1
		1	D40[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	1	0	1	0	0	0	0

SETDGCLUT continues to the next page.

(6)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0
C1	SETDGCLUT	1	D41[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	0	0	0	0	0	0	0
		1	D42[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	0	0	0	0	0	0	0
		1	D43[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	1	1	0	1	0	1	0
		1	D44[7:0]							
	initial	-	0	0	0	0	1	0	0	0
	recommend	-	1	1	0	0	1	1	1	1
		1	D45[7:0]							
	initial	-	0	0	0	1	0	0	0	0
	recommend	-	1	0	1	0	1	0	0	0
		1	D46[7:0]							
	initial	-	0	0	0	1	1	0	0	0
	recommend	-	1	0	0	0	0	0	0	1
		1	D47[7:0]							
	initial	-	0	0	1	0	0	0	0	0
	recommend	-	0	1	0	1	1	1	1	1
		1	D48[7:0]							
	initial	-	0	0	1	0	1	0	0	0
	recommend	-	0	0	1	1	1	1	1	0
		1	D49[7:0]							
	initial	-	0	0	1	1	0	0	0	0
	recommend	-	0	0	1	0	0	1	0	1
		1	D50[7:0]							
	initial	-	0	0	1	1	1	0	0	0
	recommend	-	0	0	0	0	0	1	1	0
		1	D51[7:0]							
	initial	-	0	1	0	0	0	0	0	0
	recommend	-	0	0	0	0	0	0	0	0
		1	D52[7:0]							
	initial	-	0	1	0	0	1	0	0	0
	recommend	-	1	1	0	1	0	0	0	0
		1	D53[7:0]							
	initial	-	0	1	0	1	0	0	0	0
	recommend	-	1	0	1	1	0	0	1	1
		1	D54[7:0]							
	initial	-	0	1	0	1	1	0	0	0
	recommend	-	1	0	0	1	0	1	1	1
		1	D55[7:0]							
	initial	-	0	1	1	0	0	0	0	0
	recommend	-	0	1	1	1	1	1	1	1
		1	D56[7:0]							
	initial	-	0	1	1	0	1	0	0	0
	recommend	-	0	1	1	0	0	1	0	1
		1	D57[7:0]							
	initial	-	0	1	1	1	0	0	0	0
	recommend	-	0	1	0	0	1	0	1	0
		1	D58[7:0]							
	initial	-	0	1	1	1	1	0	0	0
	recommend	-	0	0	1	0	1	1	1	1

SETDGCLUT continues to the next page.

(7)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0
C1	SETDGCLUT	1	D59[7:0]							
	initial	-	1	0	0	0	0	0	0	0
	recommend	-	0	0	0	1	0	1	1	0
		1	D60[7:0]							
	initial	-	1	0	0	0	1	0	0	0
	recommend	-	1	1	1	1	1	1	0	1
		1	D61[7:0]							
	initial	-	1	0	0	1	0	0	0	0
	recommend	-	0	0	0	1	0	0	0	0
		1	D62[7:0]							
	initial	-	1	0	0	1	1	0	0	0
	recommend	-	1	1	0	0	1	0	1	0
		1	D63[7:0]							
	initial	-	1	0	1	0	0	0	0	0
	recommend	-	1	0	1	0	1	1	1	1
		1	D64[7:0]							
	initial	-	1	0	1	0	1	0	0	0
	recommend	-	1	0	0	1	1	0	0	1
		1	D65[7:0]							
	initial	-	1	0	1	1	0	0	0	0
	recommend	-	0	1	1	1	0	1	0	0
		1	D66[7:0]							
	initial	-	1	0	1	1	1	0	0	0
	recommend	-	0	1	0	0	0	0	1	1
		1	D67[7:0]							
	initial	-	1	1	0	0	0	0	0	0
	recommend	-	0	0	1	0	1	1	0	0
		1	D68[7:0]							
	initial	-	1	1	0	0	1	0	0	0
	recommend	-	0	0	0	0	1	0	0	1
		1	D69[7:0]							
	initial	-	1	1	0	1	0	0	0	0
	recommend	-	1	1	1	1	0	0	0	1
		1	D70[7:0]							
	initial	-	1	1	0	1	1	0	0	0
	recommend	-	1	1	0	1	0	0	1	1
		1	D71[7:0]							
	initial	-	1	1	1	0	0	0	0	0
	recommend	-	1	1	0	0	0	0	0	1
		1	D72[7:0]							
	initial	-	1	1	1	0	1	0	0	0
	recommend	-	1	0	1	0	0	0	1	0
		1	D73[7:0]							
	initial	-	1	1	1	1	0	0	0	0
	recommend	-	0	1	1	0	1	0	1	1
		1	D74[7:0]							
	initial	-	1	1	1	1	1	0	0	0
	recommend	-	0	0	0	1	0	0	0	0
		1	D75[7:0]							
	initial	-	1	1	1	1	1	1	1	1
	recommend	-	0	0	0	0	0	0	0	0
		1	D76[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	1	1	1	1	1	1	1

SETDGCLUT continues to the next page.

(8)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0
C1	SETDGCLUT	1	D77[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	1	1	1	1	1	1	1
		1	D78[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	0	1	0	1	0	1	0
		1	D79[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	0	1	0	1	0	1	0
		1	D80[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	0	0	1	0	0	0	1
		1	D81[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	1	0	1	0	1	0	1
		1	D82[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	1	0	1	0	0	0	0
		1	D83[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	0	0	0	0	0	0	0
		1	D84[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	0	0	0	0	0	0	0
		1	D85[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	0	0	0	0	0	0	0
		1	D86[7:0]							
	initial	-	0	0	0	0	1	0	0	0
	recommend	-	1	1	0	0	1	0	0	1
		1	D87[7:0]							
	initial	-	0	0	0	1	0	0	0	0
	recommend	-	1	0	0	1	1	1	0	0
		1	D88[7:0]							
	initial	-	0	0	0	1	1	0	0	0
	recommend	-	0	1	1	1	0	1	1	1
		1	D89[7:0]							
	initial	-	0	0	1	0	0	0	0	0
	recommend	-	0	1	0	1	0	0	1	1
		1	D90[7:0]							
	initial	-	0	0	1	0	1	0	0	0
	recommend	-	0	0	1	1	0	1	0	0
		1	D91[7:0]							
	initial	-	0	0	1	1	0	0	0	0
	recommend	-	0	0	0	1	1	1	0	0
		1	D92[7:0]							
	initial	-	0	0	1	1	1	0	0	0
	recommend	-	1	1	1	1	1	0	1	1
		1	D93[7:0]							
	initial	-	0	1	0	0	0	0	0	0
	recommend	-	0	0	1	0	0	0	0	0
		1	D94[7:0]							
	initial	-	0	1	0	0	1	0	0	0
	recommend	-	1	1	0	0	0	1	0	1

SETDGCLUT continues to the next page.

(9)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0
C1	SETDGCLUT	1	D95[7:0]							
	initial	-	0	1	0	1	0	0	0	0
	recommend	-	1	0	1	0	1	0	1	0
		1	D96[7:0]							
	initial	-	0	1	0	1	1	0	0	0
	recommend	-	1	0	0	0	1	1	0	0
		1	D97[7:0]							
	initial	-	0	1	1	0	0	0	0	0
	recommend	-	0	1	1	1	0	0	1	1
		1	D98[7:0]							
	initial	-	0	1	1	0	1	0	0	0
	recommend	-	0	1	0	1	1	0	0	1
		1	D99[7:0]							
	initial	-	0	1	1	1	0	0	0	0
	recommend	-	0	1	0	0	0	0	0	1
		1	D100[7:0]							
	initial	-	0	1	1	1	1	0	0	0
	recommend	-	0	0	1	0	1	0	0	0
		1	D101[7:0]							
	initial	-	1	0	0	0	0	0	0	0
	recommend	-	0	0	0	1	0	0	0	0
		1	D102[7:0]							
	initial	-	1	0	0	0	1	0	0	0
	recommend	-	1	1	1	1	0	1	1	0
		1	D103[7:0]							
	initial	-	1	0	0	1	0	0	0	0
	recommend	-	1	1	0	1	1	1	0	0
		1	D104[7:0]							
	initial	-	1	0	0	1	1	0	0	0
	recommend	-	1	1	0	0	0	1	0	0
		1	D105[7:0]							
	initial	-	1	0	1	0	0	0	0	0
	recommend	-	1	0	1	0	1	0	1	0
		1	D106[7:0]							
	initial	-	1	0	1	0	1	0	0	0
	recommend	-	1	0	0	1	0	0	1	1
		1	D107[7:0]							
	initial	-	1	0	1	1	0	0	0	0
	recommend	-	0	1	1	0	1	0	1	0
		1	D108[7:0]							
	initial	-	1	0	1	1	1	0	0	0
	recommend	-	0	1	0	0	0	0	0	0
		1	D109[7:0]							
	initial	-	1	1	0	0	0	0	0	0
	recommend	-	0	0	1	0	0	1	0	1
		1	D110[7:0]							
	initial	-	1	1	0	0	1	0	0	0
	recommend	-	0	0	0	0	0	0	0	0
		1	D111[7:0]							
	initial	-	1	1	0	1	0	0	0	0
	recommend	-	1	1	1	0	1	0	0	0
		1	D112[7:0]							
	initial	-	1	1	0	1	1	0	0	0
	recommend	-	1	1	0	0	1	0	1	0

SETDGCLUT continues to the next page.

(10)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0
C1	SETDGCLUT	1	D113[7:0]							
	initial	-	1	1	1	0	0	0	0	0
	recommend	-	1	0	1	1	0	1	1	1
		1	D114[7:0]							
	initial	-	1	1	1	0	1	0	0	0
	recommend	-	1	0	0	1	1	1	0	0
		1	D115[7:0]							
	initial	-	1	1	1	1	0	0	0	0
	recommend	-	0	0	0	1	1	0	1	0
		1	D116[7:0]							
	initial	-	1	1	1	1	1	0	0	0
	recommend	-	0	0	0	0	0	1	0	1
		1	D117[7:0]							
	initial	-	1	1	1	1	1	1	1	1
	recommend	-	0	0	0	0	0	0	0	0
		1	D118[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	0	1	1	1	1	1	1
		1	D119[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	1	1	1	1	1	1	0
		1	D120[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	0	1	0	1	0	1	0
		1	D121[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	0	1	0	1	0	1	0
		1	D122[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	1	0	0	1	0	1	0	1
		1	D123[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	1	0	1	0	1	0	1
		1	D124[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	1	0	1	0	0	0	0
		1	D125[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	0	0	0	0	0	0	0
		1	D126[7:0]							
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	0	0	0	0	0	0	0
CC	SETDGCLUT	0	1	1	0	0	1	1	0	0
		1	-	-	-	SM_PANEL	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL
	initial	-	0	0	0	0	0	0	0	0
	recommend	-	0	0	0	1	1	0	0	0

(11)

(Hex)	Register		DNC	D7	D6	D5	D4	D3	D2	D1	D0
E0	SET SIP READ INDEX		0	1	1	1	0	0	0	0	0
			1	-	-	G1_VRP0[5:0]					
		initial	-	0	0	0	0	0	1	0	1
		recommend	1	0	0	0	0	0	0	1	1
			1	G1_CGMP0[1:0]		G1_VRP1[5:0]					
		initial	-	0	0	0	1	0	0	0	1
		recommend	1	0	1	0	0	1	0	0	1
			1	G1_CGMP1[1:0]		G1_VRP2[5:0]					
		initial	-	0	0	0	1	0	1	0	1
		recommend	1	0	1	0	0	1	1	1	0
			1	G1_CGMP2[1:0]		G1_VRP3[5:0]					
		initial	-	0	0	1	0	0	1	0	0
		recommend	1	0	1	0	0	1	1	0	0
			1	G1_CGMP3[1:0]		G1_VRP4[5:0]					
		initial	-	0	0	1	0	0	1	1	1
		recommend	1	0	1	0	1	0	1	1	1
			1	G1_CGMP5	G1_CGMP4	G1_VRP5[5:0]					
		initial	-	0	0	1	0	0	1	1	1
		recommend	1	1	1	1	1	0	1	0	0
			1	-	G1_PRP0[6]	-	G1_PKP0[4:0]				
		initial	-	0	0	0	0	0	1	1	0
		recommend	1	0	0	0	0	1	0	1	1
			1	G1_PRP0[5:4]		-	G1_PKP1[4:0]				
		initial	-	1	0	0	0	1	1	0	1
		recommend	1	0	1	0	0	1	1	1	0
			1	G1_PRP0[3:2]		-	G1_PKP2[4:0]				
		initial	-	0	0	0	1	0	0	0	1
		recommend	1	0	1	0	1	0	0	1	0
			1	G1_PRP0[1:0]		-	G1_PKP3[4:0]				
		initial	-	1	1	0	1	0	1	0	1
		recommend	-	1	0	0	1	0	1	1	1
			1	-	G1_PRP1[6]	-	G1_PKP4[4:0]				
		initial	-	0	0	0	1	1	0	0	1
		recommend	-	0	0	0	1	1	0	1	0
			1	G1_PRP1[5:4]		-	G1_PKP5[4:0]				
		initial	-	1	1	0	1	0	1	1	0
		recommend	-	0	1	0	1	1	0	0	1
			1	G1_PRP1[3:2]		-	G1_PKP6[4:0]				
		initial	-	1	0	0	1	0	1	1	1
		recommend	-	1	1	0	1	0	1	1	0
			1	G1_PRP1[1:0]		-	G1_PKP7[4:0]				
		initial	-	0	0	0	0	1	0	0	1
		recommend	-	1	0	0	0	1	1	0	0
			1	-		G1_PKP8[4:0]					
		initial	-	0	0	0	0	1	0	0	1
		recommend	-	0	0	0	1	0	0	0	0
			1	-		G1_VRN0[5:0]					
		initial	-	0	0	0	0	0	1	0	1
		recommend	-	0	0	0	0	0	0	0	1
			1	G1_CGMN0[1:0]		G1_VRN1[5:0]					
		initial	-	0	0	0	1	0	0	0	1
		recommend	-	0	1	0	0	0	1	1	1

SET SPI READ INDEX continues to the next page.

(12)

(Hex)	Register	DNC	D7	D6	D5	D4	D3	D2	D1	D0
		1	G1_CGMN1[1:0]		G1_VRN2[5:0]					
	initial	-	0	0	0	1	0	1	0	1
	recommend	-	0	1	0	0	1	1	0	1
		1	G1_CGMN2[1:0]		G1_VRN3[5:0]					
	initial	-	0	0	1	0	0	1	0	0
	recommend	-	0	1	0	1	0	1	1	1
		1	G1_CGMN3[1:0]		G1_VRN4[5:0]					
	initial	-	0	0	1	0	0	1	1	1
	recommend	-	0	1	1	0	0	0	1	0
		1	G1_CGMN5	G1_CGMN4	G1_VRN5[5:0]					
	initial	-	0	0	1	0	0	1	1	1
	recommend	-	1	1	1	1	1	1	1	1
		1	-	G1_PRN0[6]	-	G1_PKN0[4:0]				
	initial	-	0	0	0	0	0	1	1	0
	recommend	-	0	0	0	0	1	0	1	0
		1	G1_PRN0[5:4]		-	G1_PKN1[4:0]				
	initial	-	1	0	0	0	1	1	0	1
	recommend	-	0	1	0	0	1	1	1	0
		1	G1_PRN0[3:2]		-	G1_PKN2[4:0]				
	initial	-	0	0	0	1	0	0	0	1
	recommend	-	0	1	0	1	0	0	0	1
		1	G1_PRN0[1:0]		-	G1_PKN3[4:0]				
	initial	-	1	1	0	1	0	1	0	1
	recommend	-	1	1	0	1	0	1	1	0
		1	-	G1_PRN1[6]	-	G1_PKN4[4:0]				
	initial	-	0	0	0	1	0	1	1	0
	recommend	-	0	0	0	1	1	0	0	1
		1	G1_PRN1[5:4]		-	G1_PKN5[4:0]				
	initial	-	1	1	0	1	0	1	1	0
	recommend	-	1	0	0	1	1	0	0	0
		1	G1_PRN1[3:2]		-	G1_PKN6[4:0]				
	initial	-	1	0	0	1	0	1	1	1
	recommend	-	0	1	0	1	0	1	1	0
		1	G1_PRN1[1:0]		-	G1_PKN7[4:0]				
	initial	-	0	0	0	0	1	0	0	1
	recommend	-	1	0	0	0	1	1	1	0
		1	-			G1_PKN8[4:0]				
	initial	-	0	0	0	0	1	0	0	1
	recommend	-	0	0	0	1	0	0	0	1
FE	SET SPI READ INDEX	0	1	1	1	1	1	1	1	0
		1	CMD_ADD[7:0]							
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
FF	SPIREAD	0	1	1	1	1	1	1	1	1
		1	CMD_DATA1[7:0]							
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
		1	...							
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-
		1	CMD_DATAN[7:0]							
	initial	-	-	-	-	-	-	-	-	-
	recommend	-	-	-	-	-	-	-	-	-

7. Sequence

Power on sequence

No.		Function	DNC	Command/Parameter
		RESETB=0		
	Wait	wait 1 msec or more		
	Power on	IOVCC, VCC on		
	Wait	wait 10 msec or more		
		RESETB=1		
	Wait	wait 10 msec or more		
	RGB signals	RGB signals start		
	Wait	wait 2 frames or more		
1	Enable extentended commands	Enable extentended commands	0	B9h
		Parameter 1	1	FFh
		Parameter 2	1	83h
		Parameter 3	1	63h
2	Set power	Set power	0	B1h
		Parameter 1	1	81h
		Parameter 2	1	24h
		Parameter 3	1	04h
		Parameter 4	1	02h
		Parameter 5	1	02h
		Parameter 6	1	03h
		Parameter 7	1	10h
		Parameter 8	1	10h
		Parameter 9	1	34h
		Parameter 10	1	3Ch
		Parameter 11	1	3Fh
		Parameter 12	1	3Fh
3	Sleep out	Sleep out	0	11h
	Wait	wait 5 msec or more		
4	Display inversion off	Display inversion off	0	20h
5	Memory access control	Memory access control	0	36h
		Parameter 1	1	00h
6	Interface pixel format	Interface pixel format	0	3Ah
		Parameter 1	1	70h
	Wail	wait 120 msec or more		
7	Set power	Set power	0	B1h
		Parameter 1	1	78h
		Parameter 2	1	24h
		Parameter 3	1	04h
		Parameter 4	1	02h
		Parameter 5	1	02h
		Parameter 6	1	03h
		Parameter 7	1	10h
		Parameter 8	1	10h
		Parameter 9	1	34h
		Parameter 10	1	3Ch
		Parameter 11	1	3Fh
		Parameter 12	1	3Fh
8	Set RGB interface related register	Set RGB interface related register	0	B3h
		Parameter 1	1	01h
9	Set display waveform cycle	Set display waveform cycle	0	B4h
		Parameter 1	1	00h
		Parameter 2	1	08h
		Parameter 3	1	6Eh
		Parameter 4	1	07h
		Parameter 5	1	01h
		Parameter 6	1	01h
		Parameter 7	1	62h
		Parameter 8	1	01h
		Parameter 9	1	57h

No.		Function	DNC	Command/Parameter
10	Set panel	Set panel	0	CCh
		Parameter 1	1	0Bh
11	Set gamma curve related setting	Set gamma curve related setting	0	E0h
		Parameter 1	1	01h
		Parameter 2	1	48h
		Parameter 3	1	4Dh
		Parameter 4	1	4Eh
		Parameter 5	1	58h
		Parameter 6	1	F6h
		Parameter 7	1	0Bh
		Parameter 8	1	4Eh
		Parameter 9	1	12h
		Parameter 10	1	D5h
		Parameter 11	1	15h
		Parameter 12	1	95h
		Parameter 13	1	55h
		Parameter 14	1	8Eh
		Parameter 15	1	11h
		Parameter 16	1	01h
		Parameter 17	1	48h
		Parameter 18	1	4Dh
		Parameter 19	1	55h
		Parameter 20	1	5Fh
		Parameter 21	1	FDh
		Parameter 22	1	0Ah
		Parameter 23	1	4Eh
		Parameter 24	1	51h
		Parameter 25	1	D3h
		Parameter 26	1	17h
		Parameter 27	1	95h
		Parameter 28	1	96h
		Parameter 29	1	4Eh
		Parameter 30	1	11h
	Wait	wait 5 msec or more		
12	Display on	Display on	0	29h

Power off sequence

No.		Function	DNC	Command/Parameter
1	Display off	Display off	0	28h
	Wait	wait 5 msec or more		
2	Sleep in	Sleep in	0	10h
	Wait	wait 2 frames or more		
3	RGB signals	RGB signals stop		

↓

Power off

Sleep sequence

No.		Function	DNC	Command/Parameter
1	Sleep in	Sleep in	0	10h
	Wait	wait 2 frames or more		
2	RGB signals	RGB signals stop		

Sleep release sequence

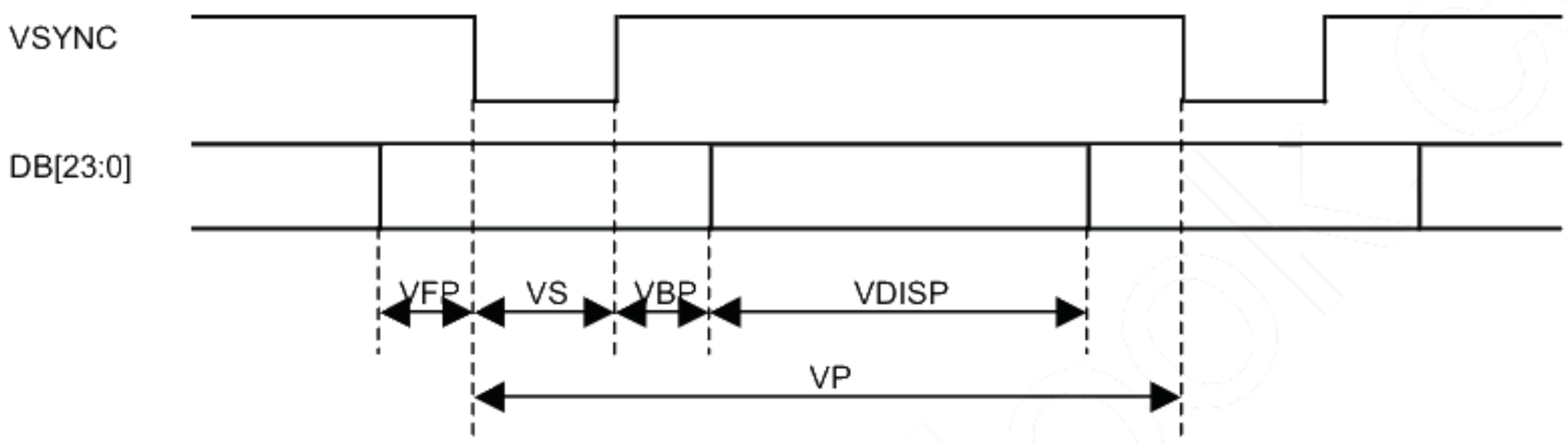
No.		Function	DNC	Command/Parameter
1	RGB signals	RGB signals start		
	Wait	wait 2 frames or more		
2	Sleep out	Sleep out	0	11h

8. RGB Interface

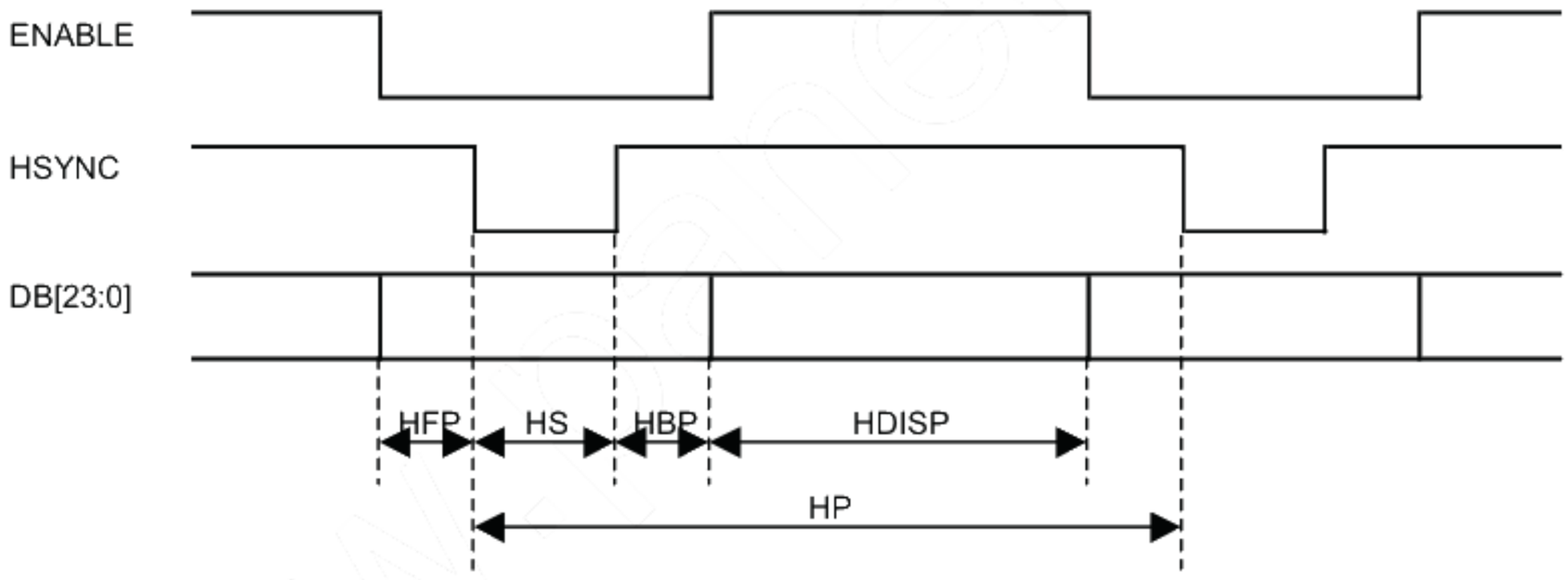
Recommended RGB interface timing

Item	Symbol	Recommended	Unit
Vertical cycle	VP	806	Line
Vertical low pulse width	VS	2	Line
Vertical front porch	VFP	2	Line
Vertical back porch	VBP	2	Line
Vertical active area	VDISP	800	Line
Vertical refresh rate	VRR	60	Hz
HS cycle	HP	508	DOTCLK
HS low pulse width	HS	10	DOTCLK
Horizontal back porch	HBP	10	DOTCLK
Horizontal front porch	HFP	8	DOTCLK
Horizontal active area	HDISP	480	MHz
Pixel clock frequency	DCK	24.576	MHz

Vertical timing



Horizontal timing



9.Absolute Maximum Ratings

Item	Symbol	Condition	Rating		Unit	Terminal
			MIN	MAX		
Power supply voltage	VCC		-0.3	4.6	V	VCC
IO logic voltage	IOVCC		-0.3	4.6	V	IOVCC
Input voltage	VI		-0.3	IOVCC+0.3	V	RESETB, SDI, SCL, CSB, VSYNC, HSYNC, DOTCLK, ENABLE, DB[23:0]
LED current	ILED		0	**	mA	VLED, LED1, ···, LEDn
Storage temperature	Tstg		-30	+80	℃	

10.Recommended Operating Conditions

Item	Symbol	Unit	Rating			Unit	Terminals
			MIN	TYP	MAX		
Supply voltage	VCC		2.6	2.7	2.8	V	VCC
IO logic voltage	IOVCC		1.7	1.8	1.9	V	IOVCC (VCC≧IOVCC)
LED current	ILED			TBD		mA	VLED, LED1, ···, LEDn
Operation temperature	Top		-20	+25	+70	C	Temperature at the surface of the display

11.Electrical Characteristics

11.1 DC Characteristics

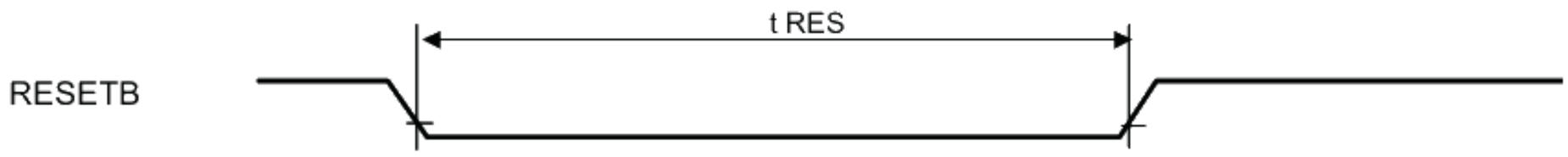
If no conditions are specified, then VCC=2.7V,IOVCC=1.8V, Ta=25℃.

Items	Symbol	Condition	Rating			Unit	Terminals
			MIN	TYP	MAX		
High level input voltage	VIH1		(0.8IOVCC)		(IOVCC)	V	RESETB, SDI, SCL, CSB, VSYNC, HSYNC, DOTCLK, ENABLE, DB[23:0]
Low level input voltage	VIL1		(0)		(0.2IOVCC)	V	
High level output voltage	VOH1	IOH=-0.1mA	(0.8IOVCC)		(IOVCC)	V	SDO
Low level output voltage	VOL1	IOL=0.1mA	(0)		(0.2IOVCC)	V	
Current Consumption	ICC1	VCC=3.0V,IOVCC=3.0V Still image *		*		mA	VCC
	ICC2	VCC=3.0V,IOVCC=3.0Vstand by		*		uA	
	IOICC1	VCC=3.0V,IOVCC=3.0V Still image *		*		mA	IOVCC
	IOICC2	VCC=3.0V,IOVCC=3.0Vstand by		*		uA	

* A still image (color bar) on display , when accessing to the driver by RGB interface mode.

11.2 AC Characteristics

RESET timing



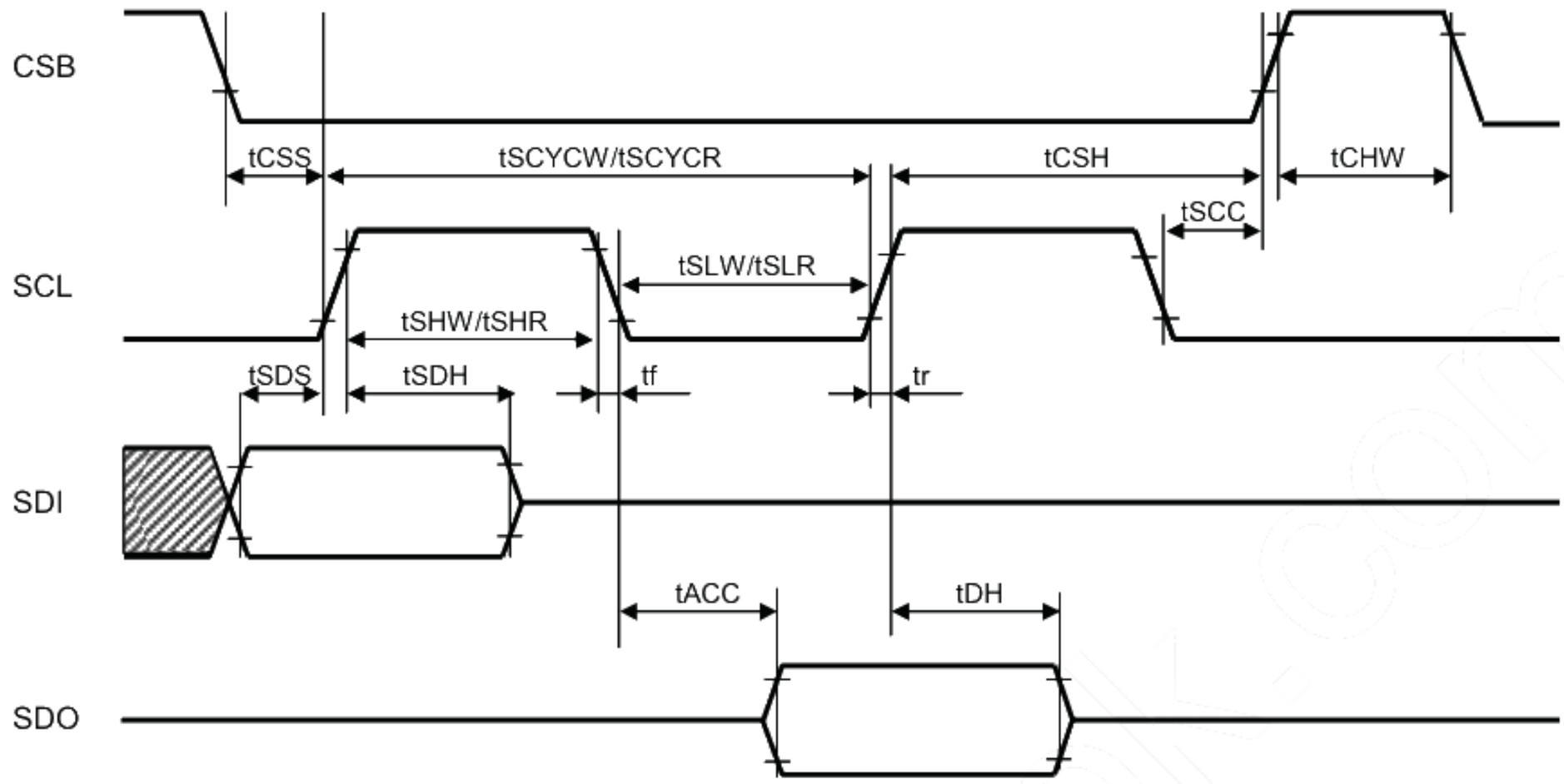
Reset low pulse width shorter than 10us do not make reset. It means undesired short pulse such as glitch, bouncing noise or electrostatic discharge do not cause irregular system reset. Please refer to the table below.

RESET timing spec

Item	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
Reset low pulse width	t RES		(10)	—	—	us

tRES Pulse	Action
Shorter than 5us	No reset
Longer than 10us	Reset
Between 5us and 10us	Not determined

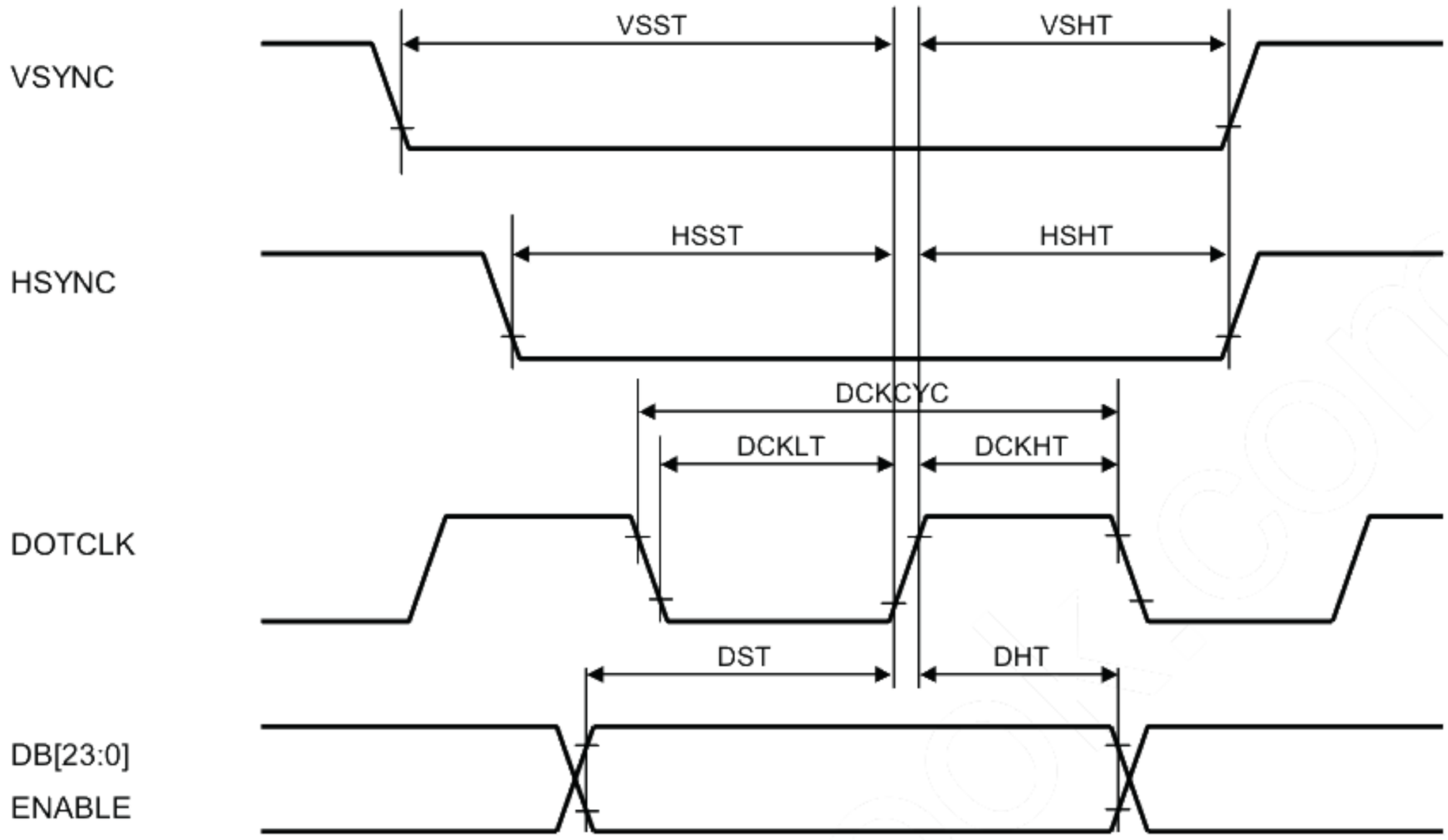
Serial Peripheral Interface(SPI)



Item	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
Serial Clock Write Cycle	tSCYCW		(100)		-	ns
Serial Clock Read Cycle	tSCYCR		(200)		-	ns
Pulse Width High at Write	tSHW		(50)		-	ns
Pulse Width High at Read	tSHR		(100)		-	ns
Pulse Width Low at Write	tSLW		(50)		-	ns
Pulse Width Low at Read	tSLR		(100)		-	ns
CSB Setup Time at Write	tCSS		(50)		-	ns
CSB Setup Time at Read	tCSS		(100)		-	ns
CSB Hold Time at Write	tSCH		(50)		-	ns
CSB Hold Time at Read	tSCH		(100)		-	ns
SDI Setup Time	tSIDS		(50)		-	ns
SDI Hold Time	tSIDH		(50)		-	ns
SDO Access Time	tSODD		(10)		(100)	ns
SDO Hold Time	tSODH		(10)		(150)	ns
Rising/Falling Time	tR, tF		-		(10)	ns

Remarks 1. All timing data is specified at 30 to 70% of VCCIO.

24 bit RGB interface



Item	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
VSYNC Setup Time	VSST		(10)	-	-	ns
VSYNC Hold Time	VSHT		(10)	-	-	ns
HSYNC Setup Time	HSST		(10)	-	-	ns
HSYNC Hold Time	HSHT		(10)	-	-	ns
DOTCLK Clock Cycle	DCKCYC	Frame Frequency= 50 to 70 Hz	(31)	-	(49.2)	ns
DOTCLK Low Time	DCKLT		(10)	-	-	ns
DOTCLK High Time	DCKHT		(10)	-	-	ns
Data Setup Time for DB[23:0]	DST		(10)	-	-	ns
Data Hold Time for DB[23:0]	DHT		(10)	-	-	ns

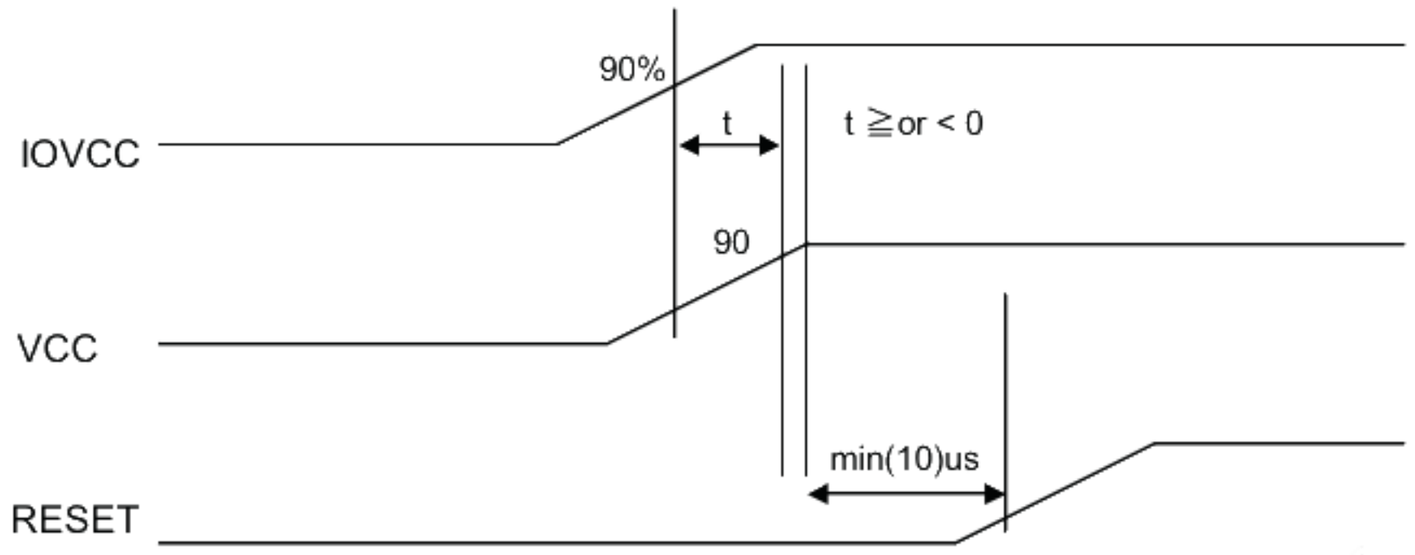
Note: (1) Signal rise and fall times are equal to or less than 20 ns.

(2) Input signals are measured by 0.30 x IOVCC for low state and 0.70 x IOVCC for high state.

12. External Power on/off Sequence

12.1 External Power On sequence

VCC and IOVCC can be applied in any order.
RESETB must be kept low for minimum (10) usec after both VCC and IOVCC have reached it's target voltage.



12.2 External Power Off sequence

VCC and IOVCC can be powered down in any order.
If the module is in "Sleep In" mode, IOVCC and VCC can be powered down minimum 0 msec after RESETB has been released.