SPECIFICATIONS № 12TLM041	Issue: Jul. 13, 2012

Specifications for

TFT-LCD Monitor

Version 1.0

MODEL COM33T3N71ZLC

Customer's Approval
Signature:
Name:
Section:
Title:
Date:

ORTUSTECH

ORTUS TECHNOLOGY CO., LTD.
Sales Dept.

Approved by

T. Tamura

Checked by

ORTUS TECHNOLOGY CO., LTD.
Product Quality Assurance

Approved by

H. Konya

Checked by

E. Iskabe

Prepared by

M. Fojo

Version History

Ver.	Date	Page	Description	
1.0	Jul. 13, 2012	-	-	First issue

Contents

1. Application ····· 4
2. Outline Specifications
   - 2.1 Features of the Product ····· 5
   - 2.2 Display Method ····· 5
3. Dimensions and Outward Form
   - 3.1 Dimensions ····· 5
   - 3.2 Outward Form ····· 6
   - 3.3 Serial Label (S-LABEL) ····· 7
4. Pin Assignment ····· 8
5. Absolute Maximum Rating ····· 9
6. Recommended Operating Conditions ····· 9
7. Characteristics
   - 7.1 DC Characteristics ····· 10
   - 7.2 Reset Timing Characteristics ····· 11
   - 7.3 AC Characteristics ····· 11
   - 7.4 Input Timing Characteristics ····· 13
   - 7.5 Input Timing Chart ····· 14
8. Block Diagram ····· 15
9. Interface
   - 9.1 RGB Interface ····· 16
   - 9.2 Serial Interface ····· 16
10. Driving Description
    - 10.1 Registers List ····· 18
    - 10.2 GRAM Address ····· 22
    - 10.3 RGB <=> Internal Clock Operation ····· 23
    - 10.4 Update Still Picture Area in Moving Picture Mode ····· 24
11. Sequence
    - 11.1 Power-ON Sequence ····· 25
    - 11.2 Power-OFF / Standby Sequence ····· 27
    - 11.3 Standby Release Sequence ····· 27
    - 11.4 Refresh Sequence 1 ····· 29
    - 11.5 Refresh Sequence 2 ····· 31
    - 11.6 Power-ON / Power-OFF Diagram ····· 33
12. Characteristics
    - 12.1 Optical Characteristics ····· 34
    - 12.2 Temperature Characteristics ····· 35
13. Criteria of Judgment
    - 13.1 Defective Display and Screen Quality ····· 36
    - 13.2 Screen and Other Appearance ····· 37
14. Reliability Test ····· 38
15. Packing Specifications ····· 40
16. Handling Instruction
    - 16.1 Cautions for Handling LCD panels ····· 41
    - 16.2 Precautions for Handling ····· 42
    - 16.3 Precautions for Operation ····· 42
    - 16.4 Storage Condition for Shipping Cartons ····· 43
    - 16.5 Precautions for Peeling off the Protective film ····· 43

APPENDIX ····· 44

1. Application

This Specification is applicable to 8.28cm (3.3 inch) TFT-LCD monitor for non-military use.

◎ ORTUS TECHNOLOGY makes no warranty or assume no liability that use of this Product and/or any information including drawings in this Specification by Purchaser is not infringing any patent or other intellectual property rights owned by third parties, and ORTUS TECHNOLOGY shall not grant to Purchaser any right to use any patent or other intellectual property rights owned by third parties. Since this Specification contains ORTUS TECHNOLOGY's confidential information and copy right, Purchaser shall use them with high degree of care to prevent any unauthorized use, disclosure, duplication, publication or dissemination of ORTUS TECHNOLOGY'S confidential information and copy right.

◎ If Purchaser intends to use this Products for an application which requires higher level of reliability and/or safety in functionality and/or accuracy such as transport equipment (aircraft, train, automobile, etc.), disaster-prevention/security equipment or various safety equipment, Purchaser shall consult ORTUS TECHNOLOGY on such use in advance.

◎ This Product shall not be used for application which requires extremely higher level of reliability and/or safety such as aerospace equipment, telecommunication equipment for trunk lines, control equipment for nuclear facilities or life-support medical equipment.

◎ ORTUS TECHNOLOGY assumes no liability for any damage resulting from misuse, abuse, and/or miss-operation of the Product deviating from the operating conditions and precautions described in the Specification.

◎ If any issue arises as to information provided in this Specification or any other information, ORTUS TECHNOLOGY and Purchaser shall discuss them in good faith and seek solution.

◎ ORTUS TECHNOLOGY assumes no liability for defects such as electrostatic discharge failure occurred during peeling off the protective film or Purchaser's assembly process.

◎ This Product is compatible for RoHS directive.

Object substance	Maximum content [ppm]
Cadmium and its compound	100
Hexavalent Chromium Compound	1000
Lead & Lead compound	1000
Mercury & Mercury compound	1000
Polybrominated biphenyl series (PBB series)	1000
Polybrominated biphenyl ether series (PBDE series)	1000

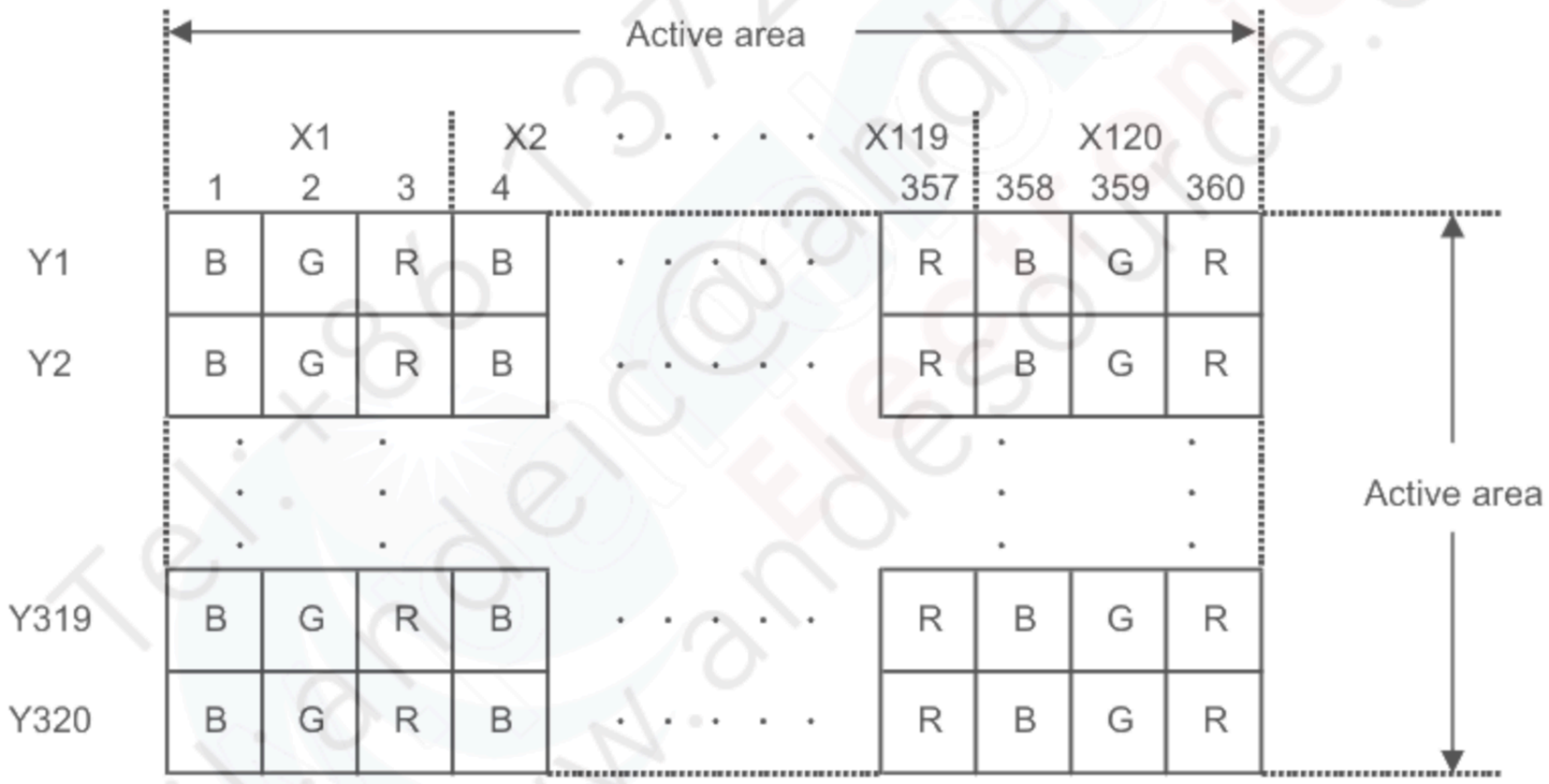
2. Outline Specifications

2.1 Features of the Product

- 3.3 inch diagonal display, 120 x RGB [H] x 320 [V] dots.
- 262,144 / 65,536 colors.
- Single power supply operation of 3.3V.
- Timing generator [TG], Counter-electrode driving circuitry, Built-in power supply circuit.
- Power save (Standby) mode capable.
- Long life & High bright white LED back-light.

2.2 Display Method

Items	Specifications	Remarks
Display type	TN type 262,144 or 65,536 colors. Transmissive type, Normally white	
Driving method	a-Si TFT Active matrix. Line-scanning, Non-interlace.	
Dot arrangement	RGB stripe arrangement.	Refer to "Dot arrangement"
Signal input method	Data : 18-bit / 16-bit RGB interface. Command : SPI interface.	
Backlight type	Long life & High bright white LED.	
Viewing direction	3:00 (Right)	



Dot arrangement (FPC cable placed right side)

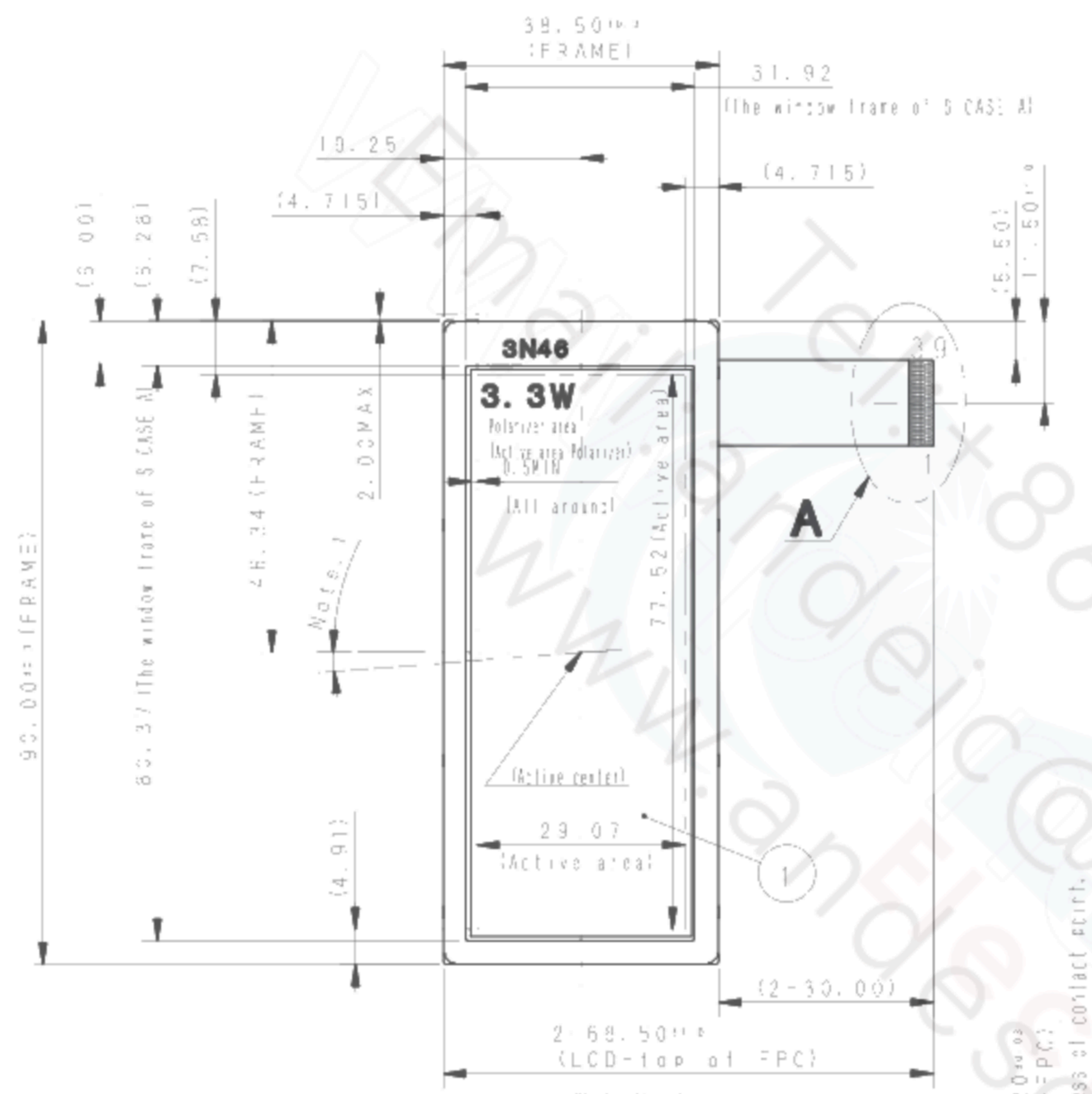
3. Dimensions and Outward Form

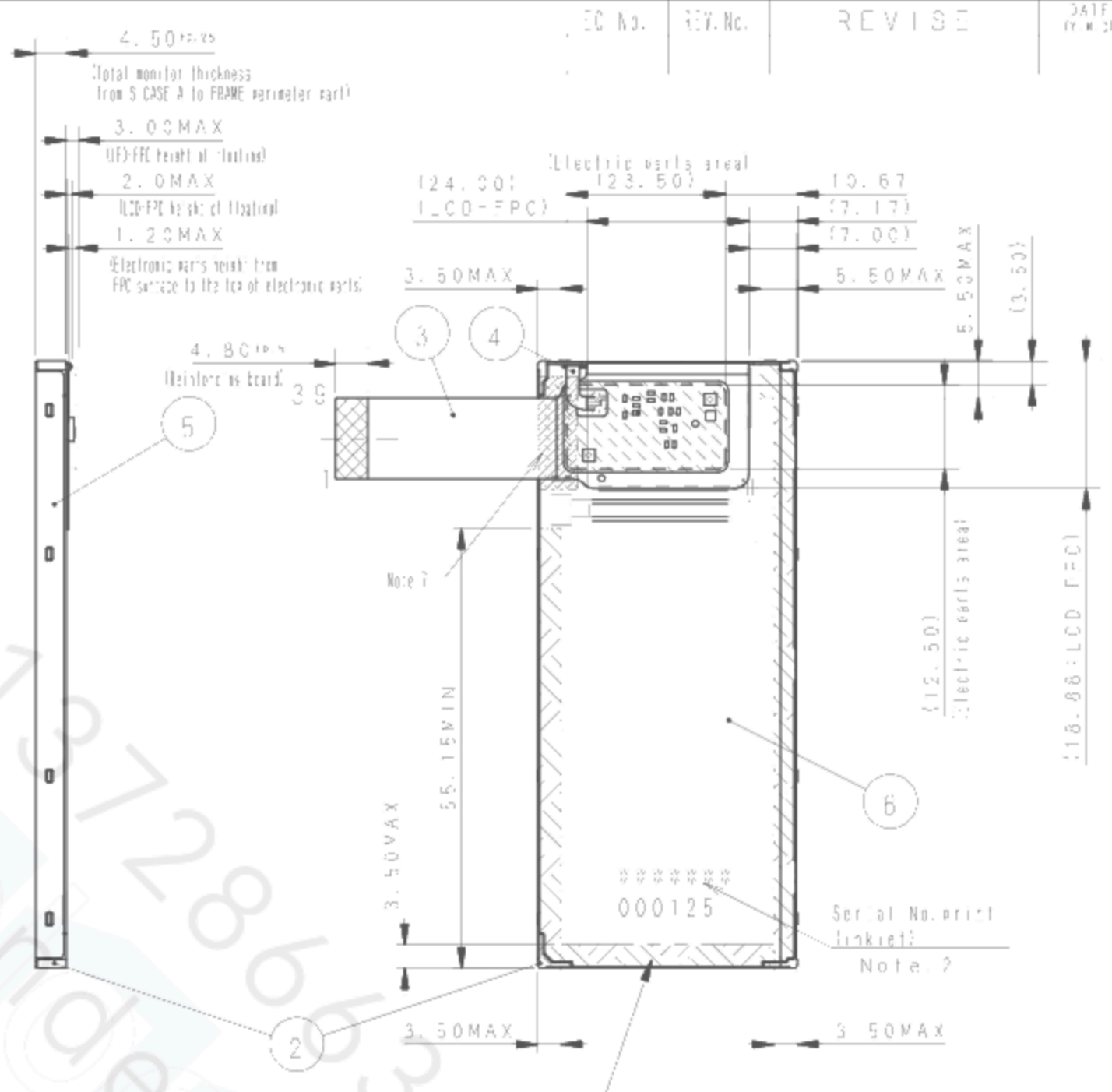
3.1 Dimensions

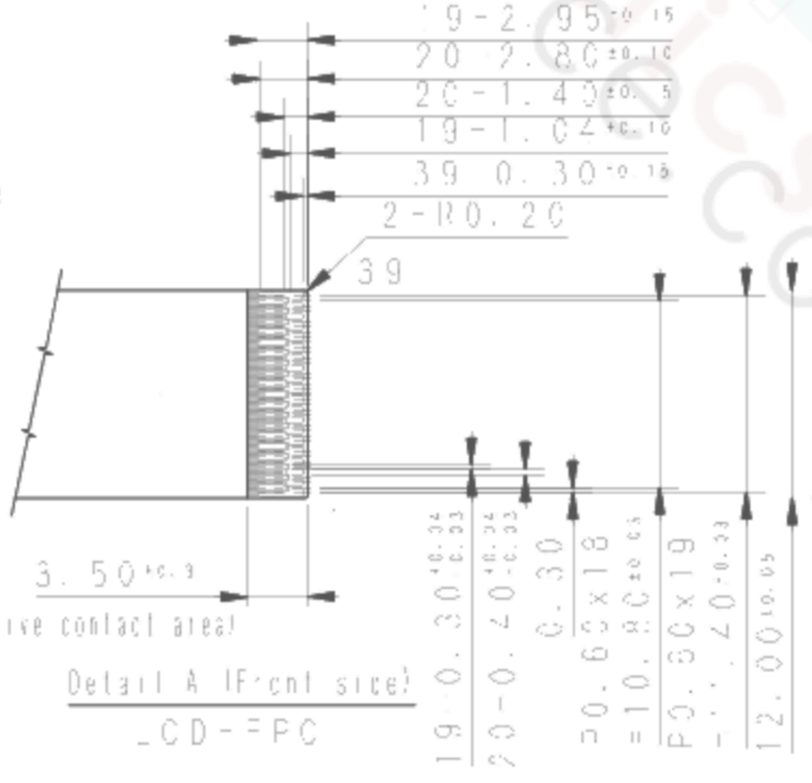
Items	Specifications	Unit	Remarks
Outline dimensions	38.5[H] × 90.0[V] × 4.50[D]	mm	Exclude FPC cable and parts on FPC.
Active area	29.07[H] × 77.52[V]	mm	8.28cm diagonal
Number of dots	360[H] × 320[V]	dot	
Dot pitch	80.75[H] × 242.25[V]	um	
Weight	26.4	g	Include FPC cable

EC No.	REV. No.	REVISE	DATE (Y.M.D)	APPROVED	CHECKED	PREPA

(6/45
12TLM04
Issue: Jul. 13, 201







Note 1. Angular deviation of LCD cell from the TFT-LCD monitor's reference axis shall be less than [1.40°].
Note 2. A serial number is printed on the part shown in figure.
Note 3. Recommended FPC connectors
Hirose part number: FH23-39S-0.3SHW(05) (Lower contact)
FPC pin assignment differs from a position of Datum Pin of recommended FPC connector.
Please notice the difference when designing your circuit with much care.
Note 4. Protective film is affixed on front surface of the parcel. Location tolerance of the protective film shall be ±1.5mm to the polarizing film.
Note 5. Burrs on the S CASE A, S CASE C must stick out outward. (The height of burrs must be 0.03mm or less.)
Note 6. Refer to "13. CRITERIA OF JUDGMENT" about the appearance specification of a polarizer.
Note 7. Height of float of LCD FPC cannot be guaranteed in ▨ area.

S CASE C	6		SUS t=0.15	
S CASE A	5		SUS t=0.15	
LED-FPC	4			
LCD-FPC	3			
FRAME	2		PC	
TFT-LCD PANEL	1		Glass substrate thickness=0.7t	
PART NAME	ITEM	PART CODE	MODEL NUMBER	REMARK

APPROVED 橋爪	GENERAL TOLERANCE	F.C.5	SCALE 1/1	UNIT mm
CHECKED 平塩	ISSUED (YY:MM:DD)	12:07:02	MODEL	COM3313N71Z000
CHECKED	NAME			
DESIGN 佐藤弘隆	OUTLINE-D3N71			
DRAW 佐藤弘隆				

ORTUSTECH
ORTUS TECHNOLOGY CO.,LTD.
DO NOT DUPLICATE, CONFIDENTIAL AND PROPRIETA

DRAWING No.	REV	SHEET
RJD524191D301		

3.3 Serial No. print (S-print)

1) Display Items

S-print indicates the least significant digit of manufacture year (1digit), manufacture month with below alphabet (1letter), model code (4characters), serial number (6digits).

* Contents of Display

*	*	****	******
a	b	c	d

	Contents of display			
a	The least significant digit of manufacture year			
b	Manufacture month	Jan-A	May-E	Sep-I
		Feb-B	Jun-F	Oct-J
		Mar-C	Jul-G	Nov-K
		Apr-D	Aug-H	Dec-L
c	Model code	33SC (Made in Japan)		
		33TC (Made in Malaysia)		
		33VC (Made in Malaysia)		
d	Serial number			

* Example of indication of Serial No. print (S-print)

・Made in Japan

2J33SC000125

means "manufactured in October 2012, 3.3" S type, C specifications, serial number 000125"

・Made in Malaysia

2J33TC000125

means "manufactured in October 2012, 3.3" T type, C specifications, serial number 000125"

・Made in China

2J33VC000125

means "manufactured in October 2012, 3.3" V type, C specifications, serial number 000125"

2) Location of Serial No. print (S-print)

Refer to 3.2 "Outward Form".

3)Others

Please note that it is likely to disappear with an organic solvent about the Serial print.

4. Pin Assignment

No.	Symbol	Function
1	BLL	LED drive power source. (Cathode side)
2	BLH	LED drive power source. (Anode side)
3	TEST1	Open
4	VCC	Power supply input.
5	VCC	Power supply input.
6	VSYNC	Vertical sync signal input. (Negative polarity at VSPL=0)
7	HSYNC	Horizontal sync signal input. (Negative polarity at HSPL=0)
8	PCLK	Clock input for display. (Data Input on the rising edge at DPL=0)
9	DE	Input data effective signal. (Lo: active at EPL=0.)
10	GND	Ground
11	RESB	System reset signal input. (Lo: active)
12	GND	Ground
13	RDB	Connect to VCC.
14	RS	Connect to VCC.
15	GND	Ground
16	GND	Ground
17	DB17	Display data input for (R). 00h for black display DB12:LSB DB17:MSB
18	DB16	
19	DB15	
20	DB14	
21	DB13	
22	DB12	
23	DB11	Display data input for (G). 00h for black display DB6:LSB DB11:MSB
24	DB10	
25	DB9	
26	DB8	
27	DB7	
28	DB6	
29	DB5	Display data input for (B). 00h for black display DB0:LSB DB5:MSB
30	DB4	
31	DB3	
32	DB2	
33	DB1	
34	DB0	
35	SDI	Data input for serial communication.
36	SDO	Data output for serial communication. (If not use, leave it open.)
37	CSB	Chip select input for serial communication. (Lo: active)
38	SCL	Clock input for serial communication. (Data Input on the rising edge.)
39	GND	Ground

- Recommended connector: HIROSE ELECTRIC [FH23-39S-0.3SHW(05)]
- Please make sure to check a consistency between pin assignment in "3.2 Outward Form" and your connector pin assignment when designing your circuit.
  Inconsistency in input signal assignment may cause a malfunction.

5. Absolute Maximum Rating

GND=0V

Item	Symbol	Condition	Rating		Unit	Applicable terminal
			MIN	MAX		
Supply voltage	VCC		-0.3	4.6	V	VCC
Input voltage for logic	VI		-0.3	VCC+0.3	V	VSYNC,HSYNC,PCLK,DE, DB[17:0],CSB,SCL,SDI,RESB
Forward current	IL		—	60.0	mA	BLH - BLL
Storage temperature range	Tstg		-30	80	℃	
Storage humidity range	Hstg	Non condensing in an environmental moisture at or less than 40 ℃ 90%RH.				

6. Recommended Operating Conditions

GND=0V

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
Supply voltage	VCC		3.0	3.3	3.6	V	VCC
Input voltage for logic	VI		0	--	VCC	V	VSYNC,HSYNC,PCLK, DE,DB[17:0],CSB, SCL,SDI,RESB
Operational temperature range	Top	Note1,2	-20	+25	+70	℃	Panel surface temperature
Operating humidity range	Hop	Ta<=40 ℃	20	--	85	%	
		Ta>40 ℃	Non condensing in an environmental moisture at or less than 40 ℃ 85%RH.				

Note1: This monitor is operable in this temperature range. With regard to optical characteristics, refer to Item 12."CHARACTERISTICS".

7. Characteristics

7.1 DC Characteristics

7.1.1 Display Module

(Unless otherwise noted, Ta=25 ℃,VCC=3.3V,GND=0V)

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
Input Signal Voltage	VIH	VCC=3.0-3.6V	0.8×VCC	--	VCC	V	VSYNC,HSYNC, PCLK,DE, DB[17:0],CSB, SCL,SDI,RESB
	VIL		0	--	0.2×VCC	V	
Operating Current	ICC	Color bar display	--	7.5	15.0	mA	VCC
Standby Current	ICCS	Other input with constant voltage	--	25	50	uA	VCC

7.1.2 Backlight

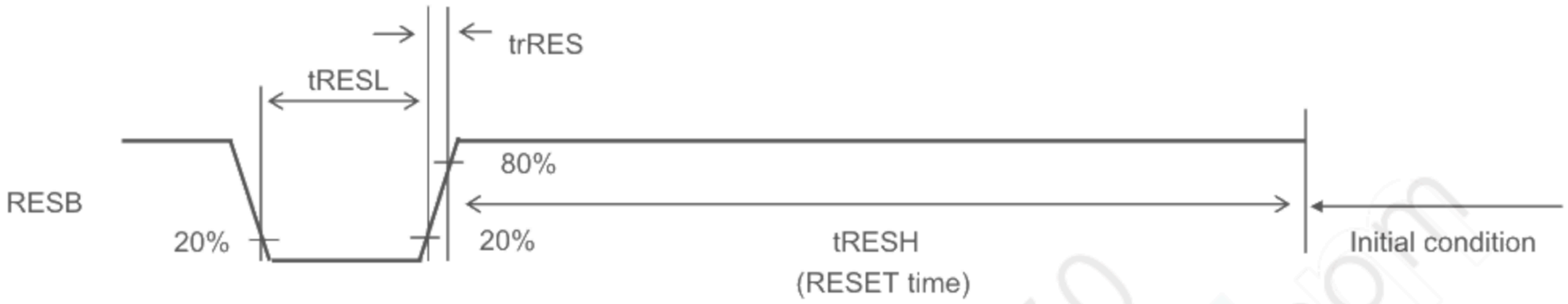
Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
Forward current	IL25	Ta=25 ℃	—	35.0	50.0	mA	BLH – BLL
Forward voltage	VL	Ta=25 ℃, IL=35.0mA	7.5	8.6	9.9	V	
Estimated Life of LED	LL	Ta=25 ℃ IL=35.0mA	—	(50,000)	—	hr	

Note: - The lifetime of the LED is defined as a period till the brightness of the LED decreases to the half of its initial value.
- This figure is given as a reference purpose only, and not as a guarantee.
- This figure is estimated for an LED operating alone. As the performance of an LED may differ when assembled as a monitor together with a TFT panel due to different environmental temperature.
- Estimated lifetime could vary on a different temperature and usually higher temperature could reduce the life significantly.

7.2 Reset Timing Characteristics

(Unless otherwise noted, Ta=25 ℃,VCC=3.3V,GND=0V)

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
RESB Low period	tRESL		1	--	--	ms	RESB
Signal Rising time	trRES		--	--	10	us	
RESB Hi period	tRESH		50	--	--	ms	

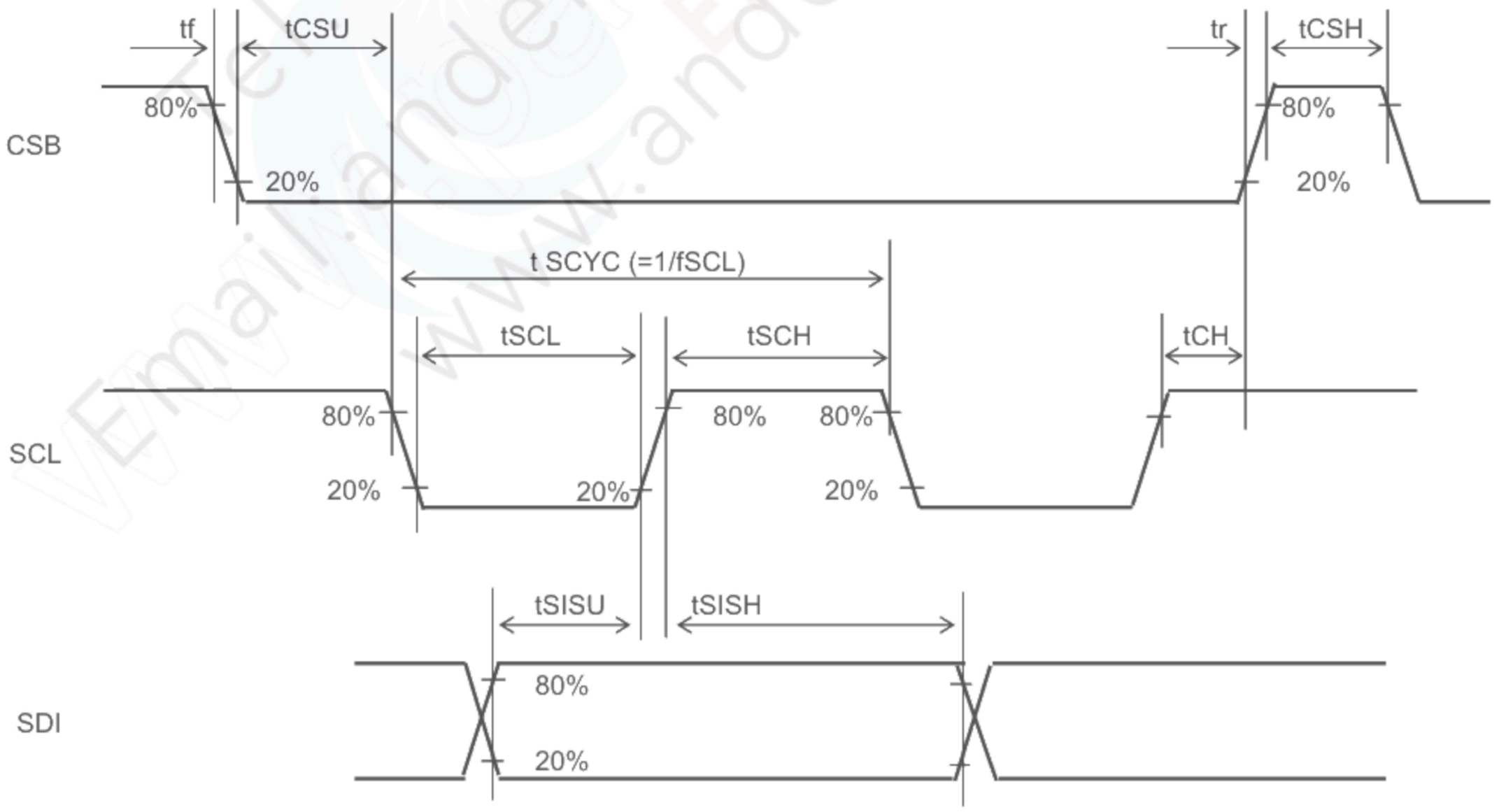


7.3 AC Characteristics

7.3.1 Serial Interface

(Unless otherwise noted, Ta=25 ℃,VCC=3.3V,GND=0V)

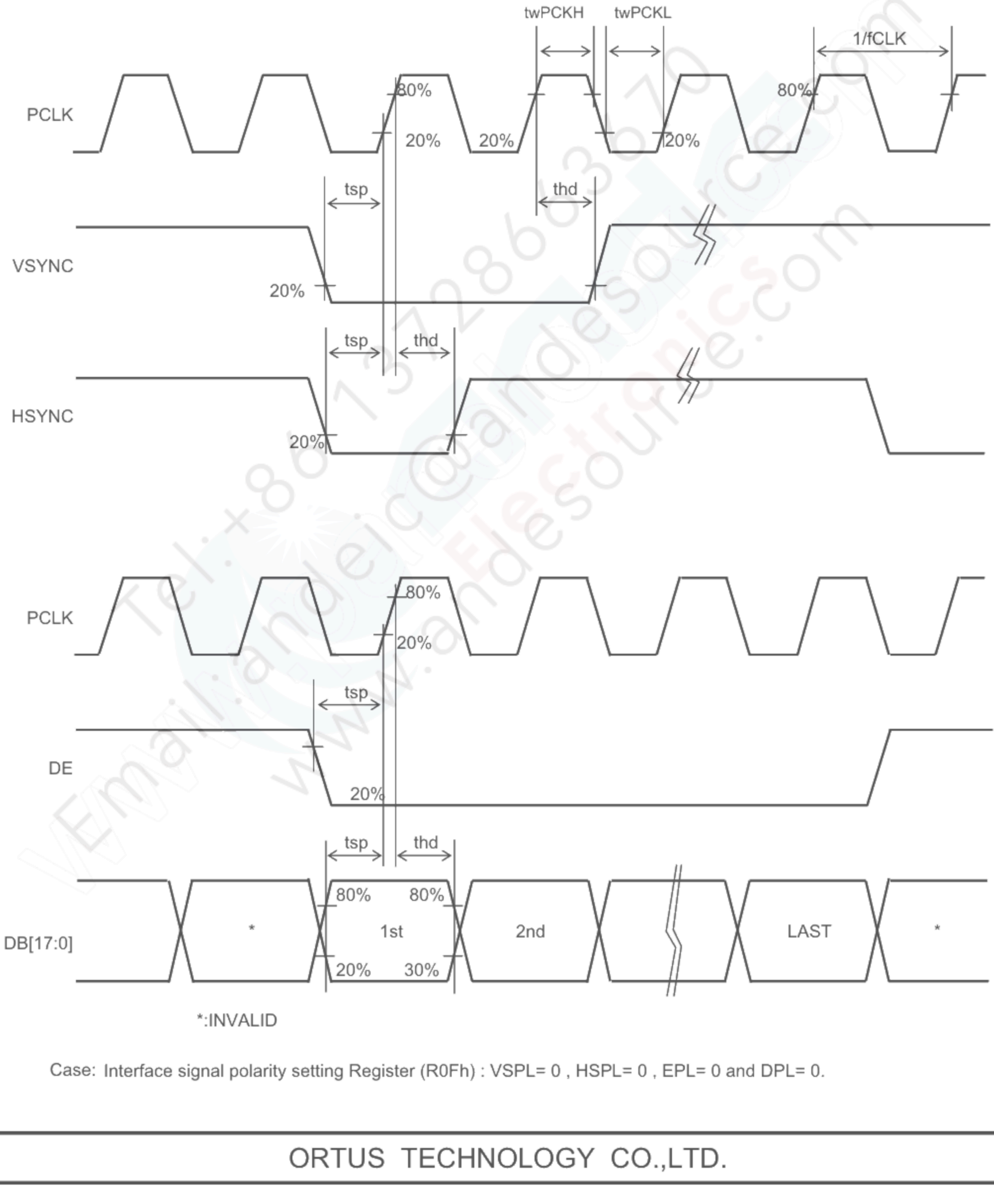
Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
Signal Rising time	tr		--	--	10	ns	CSB,SCL,SDI
Signal Falling time	tf		--	--	10	ns	
CSB setup time	tCSU		10	--	--	ns	CSB
CSB hold time	tCH		50	--	--	ns	
CSB pulse High period	tCSH		100	--	--	ns	
SDI setup time	tSISU		20	--	--	ns	SDI
SDI hold time	tSISH		20	--	--	ns	
SCL Frequency	fSCL		--	--	10	MHz	SCL
SCL pulse Low period	tSCL		40	--	--	ns	
SCL pulse High period	tSCH		40	--	--	ns	



7.3.2 RGB Interface

(Unless otherwise noted, Ta=25 ℃,VCC=3.3V,GND=0V)

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
PCLK Frequency	fCLK		--	5.0	6.6	MHz	PCLK
PCLK Low period	twPCKL	0.2×VCC or less	40	--	--	ns	
PCLK High period	twPCKH	0.8×VCC or more	40	--	--	ns	
Setup time	tsp		10	--	--	ns	PCLK,VSYNC, HSYNC,DE, DB[17:0]
Hold time	thd		40	--	--	ns	



*:INVALID

Case: Interface signal polarity setting Register (R0Fh) : VSPL= 0 , HSPL= 0 , EPL= 0 and DPL= 0.

7.4 Input Timing Characteristics

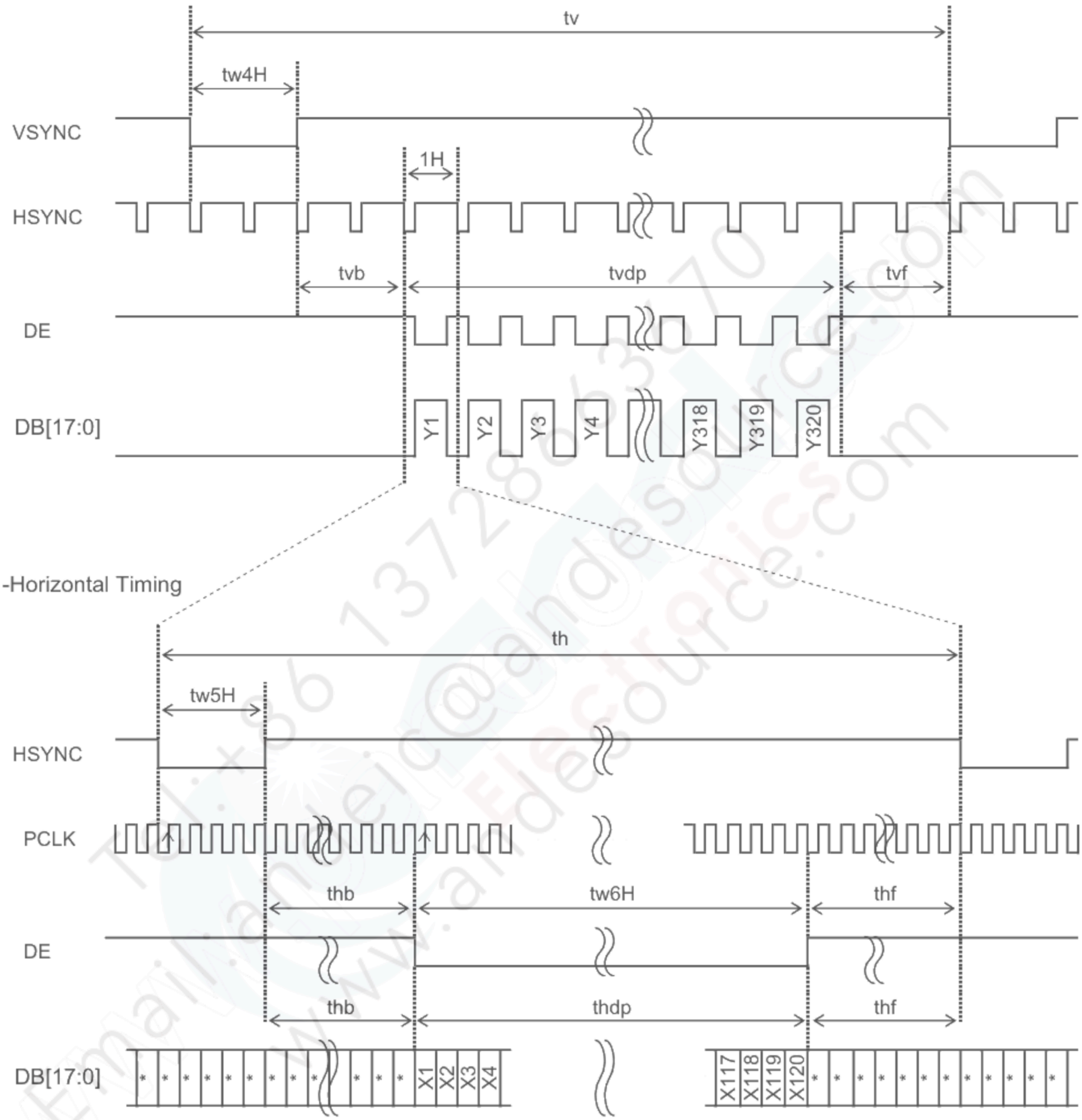
Item	Symbol	Rating			Unit	Applicable terminal
		MIN	TYP	MAX		
PCLK Frequency	fPCLK	--	5.0	6.6	MHz	PCLK
VSYNC Frequency Note	fVSYNC	54	60	66	Hz	VSYNC
VSYNC Cycle	tv	325	330	350	H	VSYNC,HSYNC
VSYNC Pulse Width	tw4H	1	2	--	H	
Vertical Back Porch	tvb	2	4	27	H	VSYNC,HSYNC,DE
Vertical Front Porch	tvf	2	4	27	H	DB[17:0]
Vertical Display Period	tvdp	--	320	--	H	
HSYNC frequency	fHSYNC	--	19.8	23.1	kHz	HSYNC
HSYNC Cycle	th	122	252	290	CLK	PCLK,HSYNC
HSYNC Pulse Width	tw5H	3	3	--	CLK	
Horizontal Back Porch	thb	2	19	250	CLK	PCLK,HSYNC,DE
Horizontal Front Porch	thf	2	110	250	CLK	DB[17:0]
DE Pulse Width	tw6H	--	120	--	CLK	PCLK,DE
Horizontal Display Period	thdp	--	120	--	CLK	PCLK,DE,DB[17:0]

Note: This is recommended spec to get high quality picture on display. It is customer's risk to use out of this frequency.

7.5 Driving Timing Chart

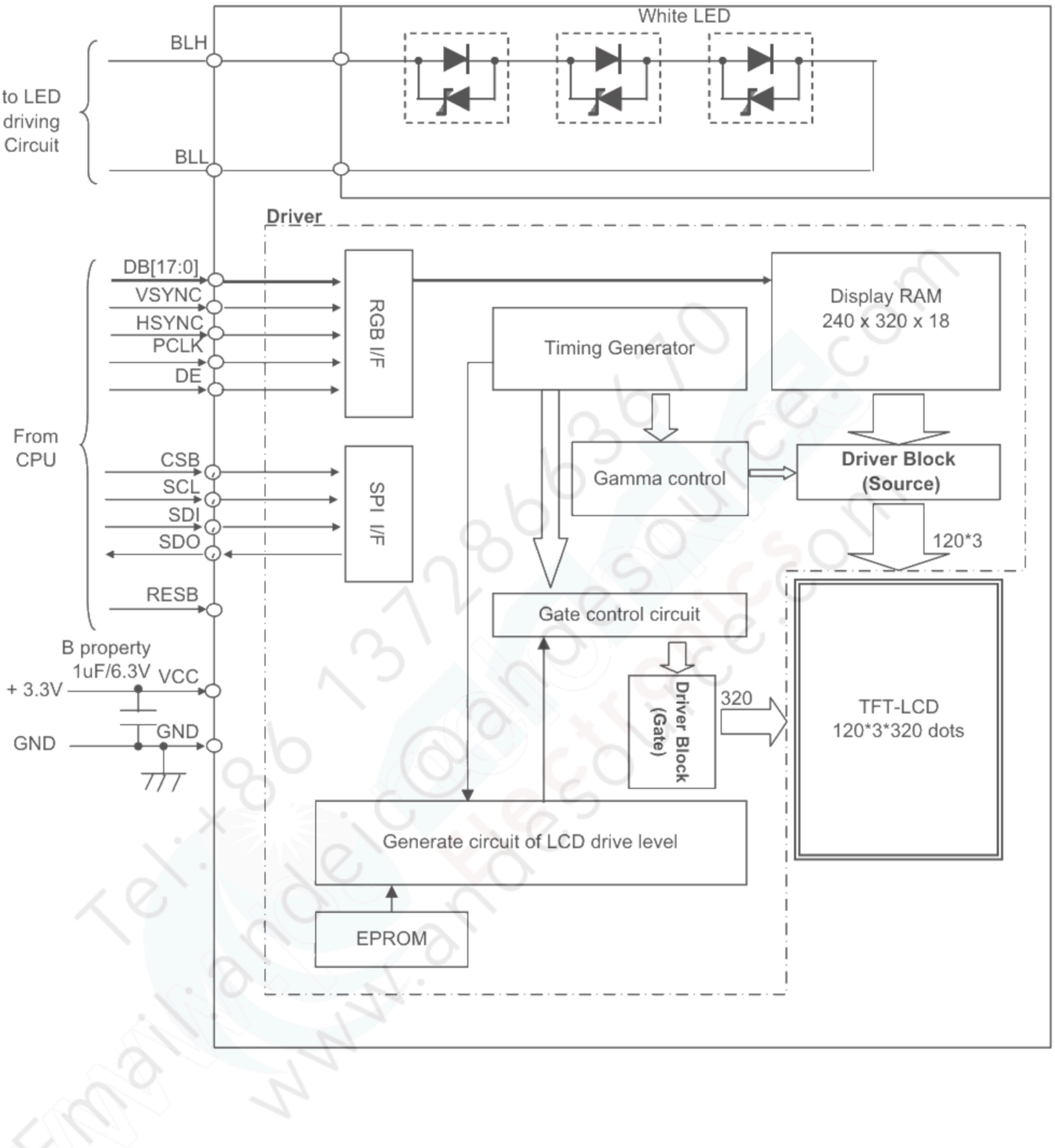
Case: Interface signal polarity setting Register (R0Fh) : VSPL= 0 , HSPL= 0 , EPL= 0 and DPL= 0.

-Vertical Timing



-Horizontal Timing

8. Block Diagram



9. Interface

9.1 RGB Interface

There are two transferring mode in RGB-I/F with the RIM[1:0] setting.
The connection method to input display data is shown below, in RGB-I/F mode .

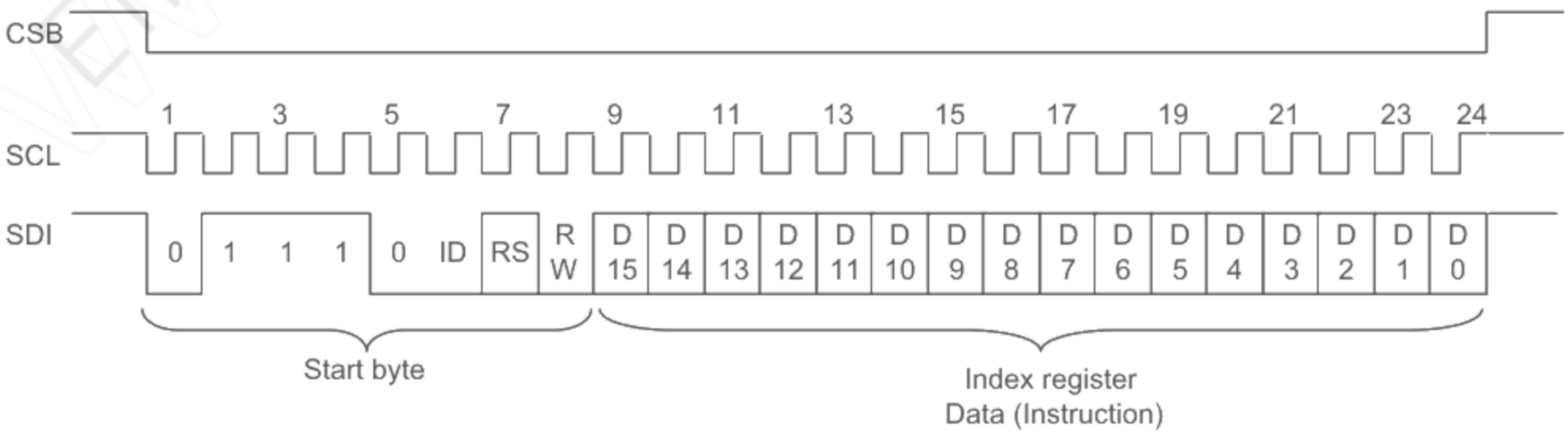
		18-bit RGB interface (R 0Ch RIM[1:0] = 00)		16-bit RGB interface (R 0Ch RIM[1:0] = 01)	
DB 17	---	R 5	Display data (R) input : MSB	R 4	Display data (R) input : MSB
DB 16	---	R 4	Display data (R) input	R 3	Display data (R) input
DB 15	---	R 3	Display data (R) input	R 2	Display data (R) input
DB 14	---	R 2	Display data (R) input	R 1	Display data (R) input
DB 13	---	R 1	Display data (R) input	R 0	Display data (R) input : LSB
DB 12	---	R 0	Display data (R) input : LSB	*	
DB 11	---	G 5	Display data (G) input : MSB	G 5	Display data (G) input : MSB
DB 10	---	G 4	Display data (G) input	G 4	Display data (G) input
DB 9	---	G 3	Display data (G) input	G 3	Display data (G) input
DB 8	---	G 2	Display data (G) input	G 2	Display data (G) input
DB 7	---	G 1	Display data (G) input	G 1	Display data (G) input
DB 6	---	G 0	Display data (G) input : LSB	G 0	Display data (G) input : LSB
DB 5	---	B 5	Display data (B) input : MSB	B 4	Display data (B) input : MSB
DB 4	---	B 4	Display data (B) input	B 3	Display data (B) input
DB 3	---	B 3	Display data (B) input	B 2	Display data (B) input
DB 2	---	B 2	Display data (B) input	B 1	Display data (B) input
DB 1	---	B 1	Display data (B) input	B 0	Display data (B) input : LSB
DB 0	---	B 0	Display data (B) input : LSB	*	

* If not use, connect it to GND.

9.2 Serial Interface

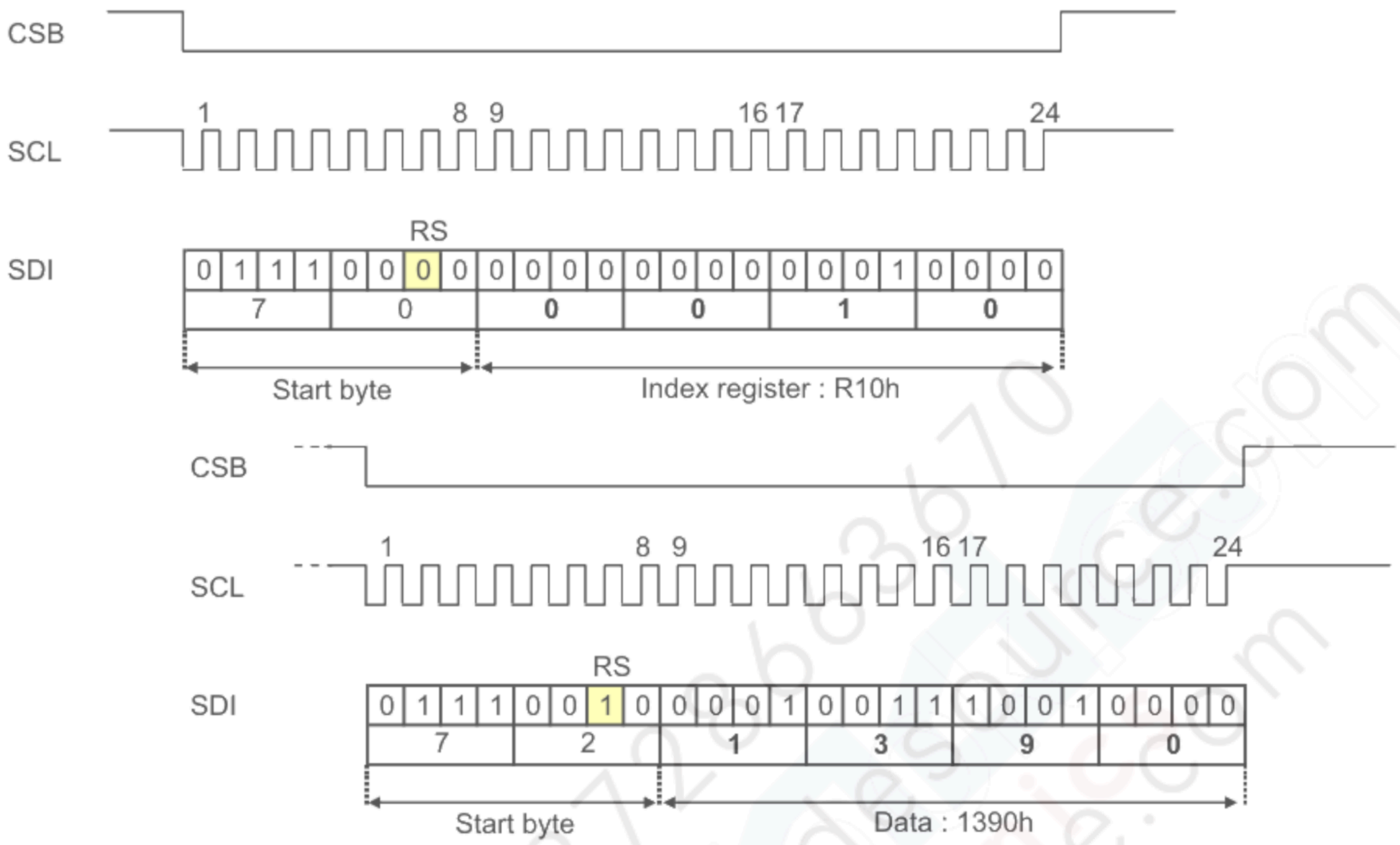
Serial communication control block consists of the chip select pin (CSB),
the serial transfer clock pin (SCL) and the serial data input pin (SDI).
The serial communication begin the transfer on the falling edge of CSB
and ends of data transfer on the rising edge of CSB.
When the initial 6bit (Start byte) is 011100, the following 16bit data is received by LSI.
The seventh data (RS bit) indicates whether the following 16bit data is "Index register " or "Data (Instruction)".
When RS=0, the following 16bit data is "Index register".
When RS=1, the following 16bit data is "Data".

9.2.1 Data format of serial communication (SPI)



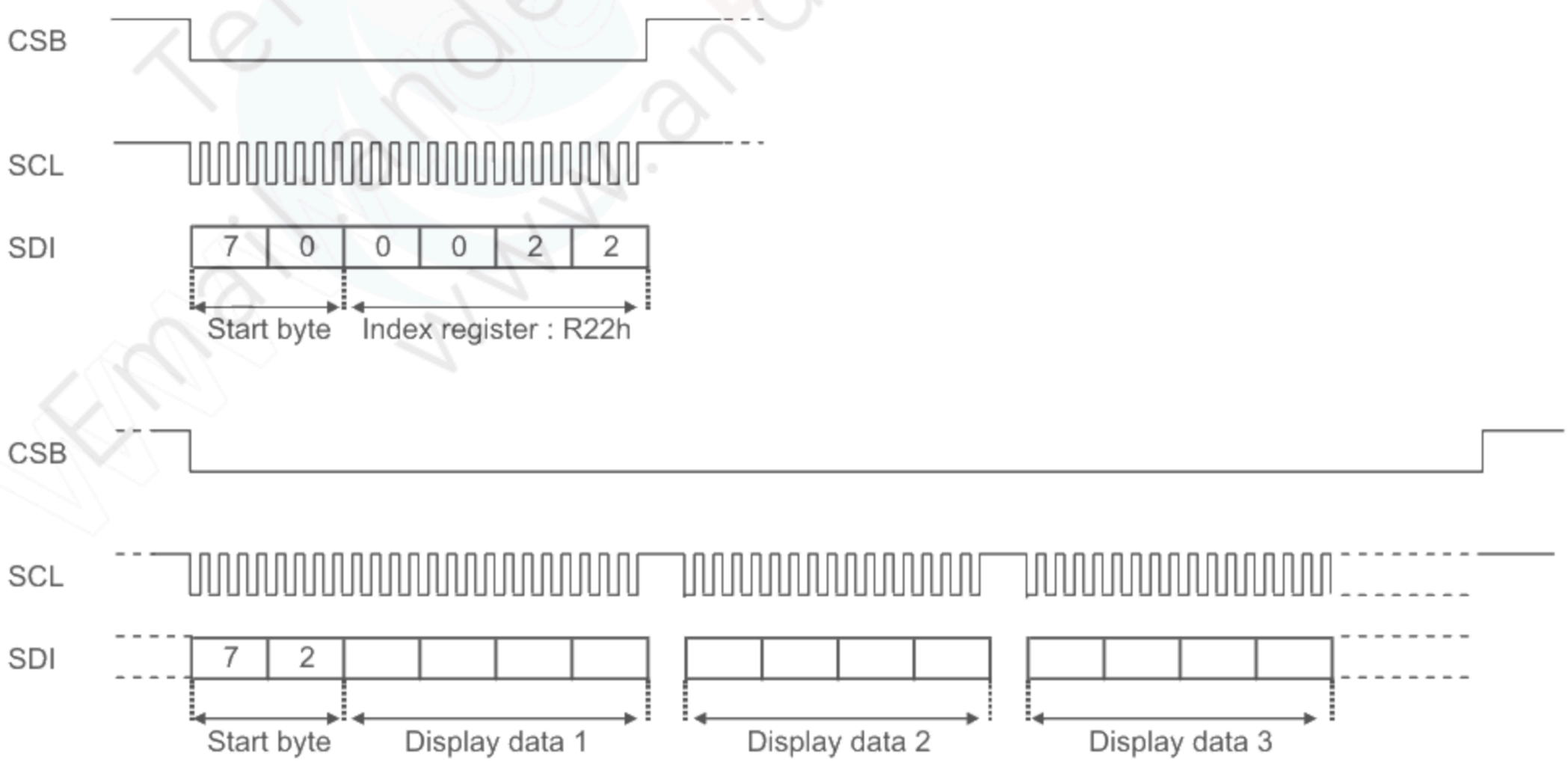
9.2.2 Register transmission

The configuration of register transmission is shown below.
EX: R10h = 0x1390h



9.2.3 Display data transmission

The configuration of 65,536 colors display data transmission in SPI mode is shown below.
Firstly, set RM=0 to start accessing GRAM via SPI.
In SPI mode, 65,536 colors display data is only transferred.



10. Driving description

10.1 Register list

(1/4)

Index	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
—	Index Register (IR)	0	0	0	0	0	0	0	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R00h	Device Code Read	1	0	0	1	0	0	1	1	0	0	1	1	0	1	0	1
		The device code "9335h" is read out when read this register.															
R01h	Driver Output Control	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
		SM: Sets the gate driver pin arrangement.															
		SS: Select the shift direction of outputs from the source driver. (0: S1 to S720)															
R02h	LCD Driving Control	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
		B/C: Sets Inversion type. (1: Line inversion)															
R03h	Entry Mode	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D1	I/D0	AM	0	0	0
		TRI/DFM: Sets data transferring method to GRAM.								ORG: Set the origin address of window area.							
		BGR: Swap the R and B order of written data.								ID/AM: Control the GRAM update method.							
R05h	16 bits data format control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EPF[1:0]	
		EPF: Sets R/B data format in 16-bit mode.															
R07h	Display Control 1	0	0	PTDE[1:0]		0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
		PTDE: Partial image enable bits.								GON/DTE: Sets the output level of Gate driver.							
		BASEE: Base image display enable bit. CL: Select 8 color mode. D: Control Source/VCOM output.															
R08h	Display Control 2	FP[7:0]								BP[7:0]							
		FP: Specify the line number of front porch period.															
		BP: Specify the line number of back porch period.															
R09h	Display Control 3	0	0	0	0	0	0	PTS[1:0]		0	0	PTG[1:0]		ISC[3:0]			
		PTS: Set the source output level in non-display area.															
		ISC: Set cycle of gate driver in non-display area. PTG: Set the scan mode in non-display area.															
R0Ah	Display Control 4	0	0	0	0	0	0	0	0	0	0	0	0	FMARK	FMI[2:0]		
		FMARK: FMARK signal output enable bit in parallel interface.															
		FMI: Set the output interval of FMARK signal.															
R0Ch	RGB Display Interface Control 1	0	ENC[2:0]			0	0	0	RM	0	0	DM[1:0]		0	0	RIM[1:0]	
		ENC: Set the GRAM write cycle in RGB-I/F. DM: Select internal clock mode and RGB-I/F mode.															
		RM: Select the interface to access the GRAM. RIM: Select the RGB-IF data width.															
R0Dh	FMARK Control	0	0	0	0	0	0	0	FMP[8:0]								
		FMP: Sets the output position of frame cycle (FMARK) .															
R0Fh	RGB Display Interface Control 2	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
		VSPL: Sets the signal polarity of VSYNC. EPL: Sets the signal polarity of DE.															
		HSPL: Sets the signal polarity of HSYNC. DPL: Sets the signal polarity of PCLK.															
R10h	Power Control 1	0	0	0	SAP	0	BT[2:0]			APE	AP[2:0]			0	0	SLP	STB
		SAP: Source Driver output enable bit. APE/AP: Power supply enable / Adjust capability.															
		BT: Select the step-up factor of VGH/VGL. SLP/STB: Sets sleep mode / standby mode.															
R11h	Power Control 2	0	0	0	0	0	DC1[2:0]			0	DC0[2:0]			0	VC[2:0]		
		DC1/0: Select the operating frequency of the step-up circuit.															
		VC: Sets the ratio factor of VCI to generate the reference voltages VCI1.															
R12h	Power Control 3	0	0	0	0	0	0	0	0	VCIRE	0	0	0	VRH[3:0]			
		VCIRE: Select the external reference voltage or internal reference voltage.															
		VRH: Set the source output VREG1OUT level.															
R13h	Power Control 4	0	0	0	VDV[4:0]					0	0	0	0	0	0	0	0
		VDV: Set the amplitude of Vcom alternating voltage.															

(2/4)

Index	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R20h	GRAM Horizontal Address Set	0	0	0	0	0	0	0	0	AD[7:0]							
		AD[7:0]: Set horizontal address of GRAM.															
R21h	GRAM Vertical Address Set	0	0	0	0	0	0	0	AD[16:8]								
		AD[16:8]: Set vertical address of GRAM.															
R22h	Write Data to GRAM	Write (Read) Data to GRAM															
R29h	Power Control 5	0	0	0	0	0	0	0	0	0	0	VCM[5:0]					
		VCM: Set the internal Vcom-DC level if OTP doesn't use.															
R2Bh	Frame Rate Control	0	0	0	0	0	0	0	0	0	0	0	0	FRS[3:0]			
		FRS: Set the Frame rate for internal CLK circuit.															
R30h	Gamma Control 1	0	0	0	0	0	KP1[2:0]			0	0	0	0	0	KP0[2:0]		
		KP0: Gamma-fine 0 adjustment register for positive polarity.															
		KP1: Gamma-fine 1 adjustment register for positive polarity.															
R31h	Gamma Control 2	0	0	0	0	0	KP3[2:0]			0	0	0	0	0	KP2[2:0]		
		KP2: Gamma-fine 2 adjustment register for positive polarity.															
		KP3: Gamma-fine 3 adjustment register for positive polarity.															
R32h	Gamma Control 3	0	0	0	0	0	KP5[2:0]			0	0	0	0	0	KP4[2:0]		
		KP4: Gamma-fine 4 adjustment register for positive polarity.															
		KP5: Gamma-fine 5 adjustment register for positive polarity.															
R35h	Gamma Control 4	0	0	0	0	0	RP1[2:0]			0	0	0	0	0	RP0[2:0]		
		RP0: Gamma-gradient 0 adjustment register for positive polarity.															
		RP1: Gamma-gradient 1 adjustment register for positive polarity.															
R36h	Gamma Control 5	0	0	0	VRP1[4:0]					0	0	0	0	VRP0[3:0]			
		VRP0: Gamma-amplitude 0 adjustment register for positive polarity.															
		VRP1: Gamma-amplitude 1 adjustment register for positive polarity.															
R37h	Gamma Control 6	0	0	0	0	0	KN1[2:0]			0	0	0	0	0	KN0[2:0]		
		KN0: Gamma-fine 0 adjustment register for negative polarity.															
		KN1: Gamma-fine 1 adjustment register for negative polarity.															
R38h	Gamma Control 7	0	0	0	0	0	KN3[2:0]			0	0	0	0	0	KN2[2:0]		
		KN2: Gamma-fine 2 adjustment register for negative polarity.															
		KN3: Gamma-fine 3 adjustment register for negative polarity.															
R39h	Gamma Control 8	0	0	0	0	0	KN5[2:0]			0	0	0	0	0	KN4[2:0]		
		KN4: Gamma-fine 4 adjustment register for negative polarity.															
		KN5: Gamma-fine 5 adjustment register for negative polarity.															
R3Ch	Gamma Control 9	0	0	0	0	0	RN1[2:0]			0	0	0	0	0	RN0[2:0]		
		RN0: Gamma-gradient 0 adjustment register for negative polarity.															
		RN1: Gamma-gradient 1 adjustment register for negative polarity.															
R3Dh	Gamma Control 10	0	0	0	VRN1[4:0]					0	0	0	0	VRN0[3:0]			
		VRN0: Gamma-amplitude 0 adjustment register for negative polarity.															
		VRN1: Gamma-amplitude 1 adjustment register for negative polarity.															

(3/4)

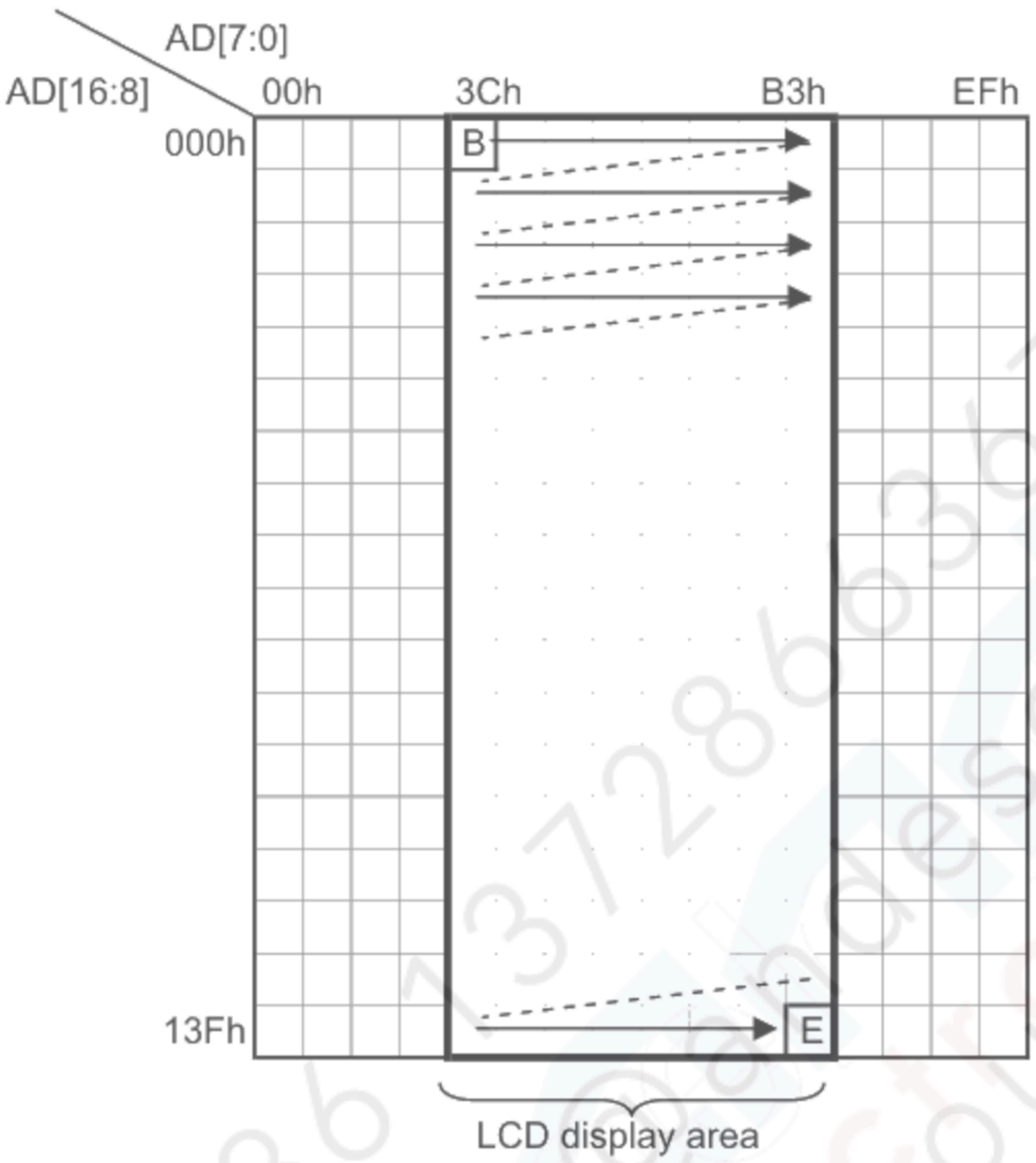
Index	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R50h	Horizontal Window Start Address	0	0	0	0	0	0	0	0	HSA[7:0]							
		HAS: Specify the horizontal address at the start of window area.															
R51h	Horizontal Window End Address	0	0	0	0	0	0	0	0	HEA[7:0]							
		HEA: Specify the horizontal address at the end of window area.															
R52h	Vertical Window Start Address	0	0	0	0	0	0	0	VSA[8:0]								
		VSA: Specify the vertical address at the start of window area.															
R53h	Vertical Window End Address	0	0	0	0	0	0	0	VEA[8:0]								
		VEA: Specify the vertical address at the end of window area.															
R60h	Display Control 5	GS	0	NL[5:0]						0	0	SCN[5:0]					
		GS: Sets the direction of gate scanning. SCN: Specify the start position of gate scanning. NL: Sets the number of lines to drive.															
R61h	Display Control 6	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
		NDL: Sets the source driver output level in the non-display area. REV: Enables the grayscale inversion. VLE: Vertical scroll display enable bit.															
R6Ah	Display Control 7	0	0	0	0	0	0	0	VL[8:0]								
		VL: Sets the scrolling amount of base image.															
R80h	Partial Image 1 Display Position	0	0	0	0	0	0	0	PTDP0[8:0]								
		PTDP0: Sets the display start position of partial image 1.															
R81h	Partial image 1 RAM Start Address	0	0	0	0	0	0	0	PTSA0[8:0]								
		PTSA0: Sets the start line address of GRAM area storing the data of partial image 1.															
R82h	Partial image 1 RAM End Address	0	0	0	0	0	0	0	PTEA0[8:0]								
		PTEA0: Sets the end line address of GRAM area storing the data of partial image 1.															
R83h	Partial Image 2 Display Position	0	0	0	0	0	0	0	PTDP1[8:0]								
		PTDP1: Sets the display start position of partial image 2.															
R84h	Partial image 2 RAM Start Address	0	0	0	0	0	0	0	PTSA1[8:0]								
		PTSA1: Sets the start line address of GRAM area storing the data of partial image 2.															
R85h	Partial image 2 RAM End Address	0	0	0	0	0	0	0	PTEA1[8:0]								
		PTEA1: Sets the end line address of GRAM area storing the data of partial image 2.															

(4/4)

Index	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R90h	Panel Interface Control 1	0	0	0	0	0	0	DIVI[1:0]		0	0	0	RTNI[4:0]				
		RTNI: Sets 1H (line) clock number in internal clock mode. DIVI: Sets the division ratio in internal clock mode.															
R92h	Panel Interface Control 2	0	0	0	0	0	NOWI[2:0]			0	0	0	0	0	0	0	0
		NOWI: Sets the gate output non-overlap period in internal clock mode.															
R95h	Panel Interface Control 3	0	0	0	0	0	0	DIVE[1:0]		0	0	0	0	0	0	0	0
		DIVE: Sets the division ratio of PCLK in RGB-I/F mode.															
R97h	Panel Interface Control 4	0	0	0	0	NOWE[3:0]				0	0	0	0	0	0	0	0
		NOWE: Sets the gate output non-overlap period in RGB-I/F mode.															
RA1h	OTP Control 1	0	0	0	0	PGMEN	0	0	0	0	0	VCM_OTP[5:0]					
		PGMEN: OTP programming enable bit. VCM_OTP: OTP programming data for VCOMH voltage.															
RA2h	OTP Control 2	PGM_CNT[1:0]		VCM_D[5:0]						0	0	0	0	0	0	0	VCMEN
		PGM_CNT: OTP programmed record. (Read only) VCMEN: OTP VCM data enable bit. VCM_D: OTP VCM data read value. (Read only)															
RA5h	OTP Control 3	KEY[15:0]															
		OTP Programming ID key protection.															
RE6h	Deep Standby Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTB
		DSTB: Set the deep standby mode.															
RE8h	TEST Register 1 (Read Only)	0	0	0	0	0	0	0	0	0	0	1	1	memwr_gnt	memwr_req	drv_gnt	drv_req
		memwr_gnt: When the LSI doesn't grant writing data to GRAM, this bit is 1. (Normal operation) memwr_req: When the LSI doesn't request writing data to GRAM, this bit is 1. (Normal operation) drv_gnt: When the LSI doesn't grant reading data from GRAM, this bit is 1. (Normal operation) drv_req: When the LSI doesn't request reading data from GRAM, this bit is 1. (Normal operation)															
REFh	TEST Register 2	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1

10.2 GRAM Address

The LSI has 240 x 320 x 18bit GRAM, and this panel uses 120 x 320 x 18bit of them as follows.
Display data is written to specified window area.



So, set address as follows when you rewrite all viewing image.

Window address	R50h	HSA[7:0] = 8'h3C
	R51h	HEA[7:0] = 8'hB3
	R52h	VSA[8:0] = 9'h000
	R53h	VEA[8:0] = 9'h13F

In the case that writing direction is normal, R03h = 16'h1030h (ID[1:0] = 11, AM = 0), set the start address is as follows.

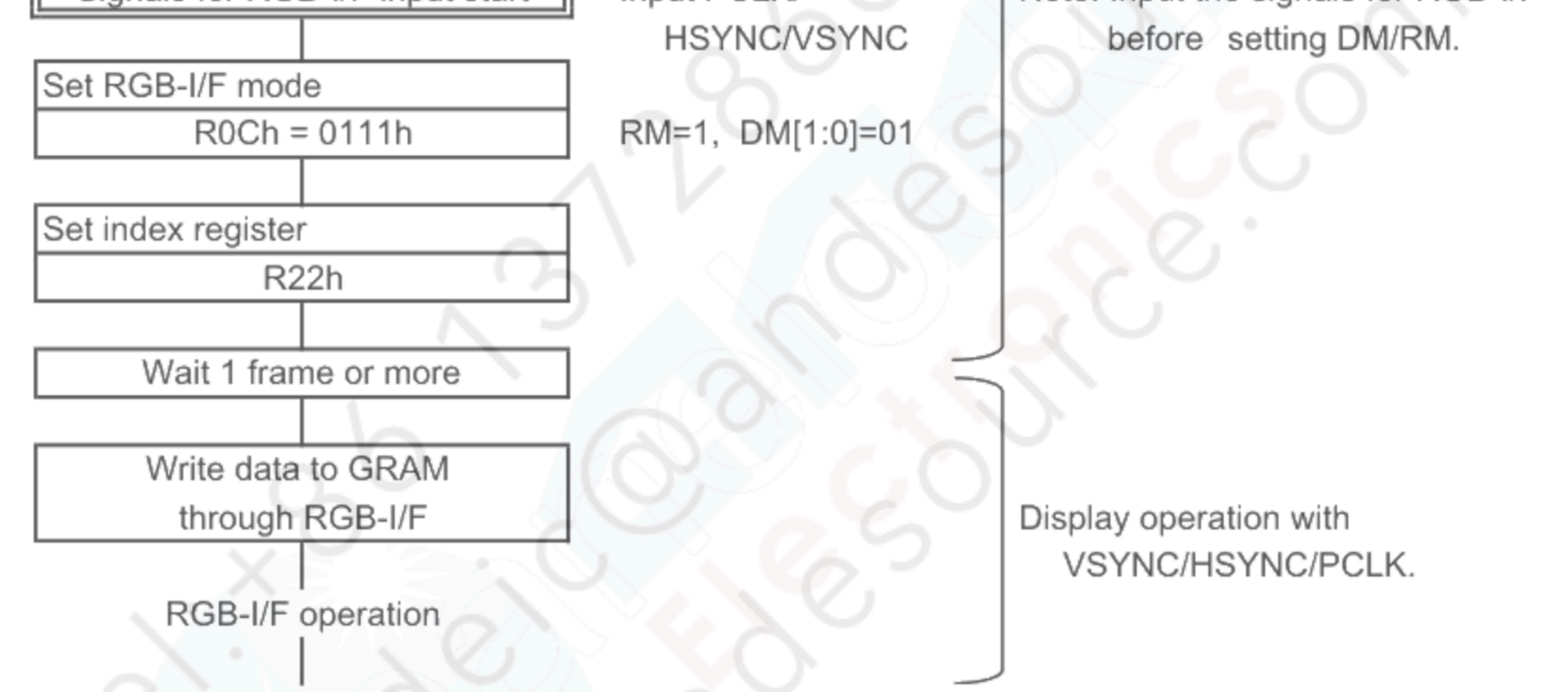
R20h	AD[7:0] = 8'h3C
R21h	AD[16:8] = 9'h000

Please make sure to set AM = 0 (Horizontal writhing direction) in RGB-I/F mode.

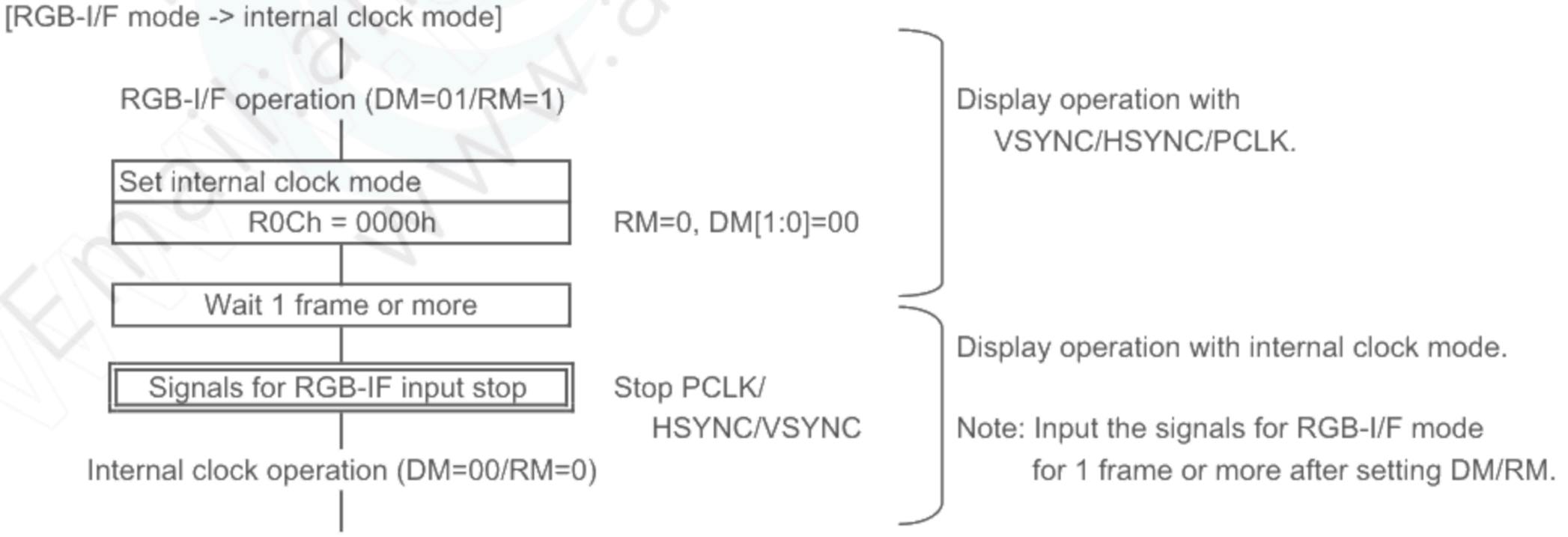
10.3 RGB <=> Internal Clock Operation

The following sequence is the method to switch between the internal clock mode and the RGB-I/F mode.

[internal clock mode -> RGB-I/F mode]



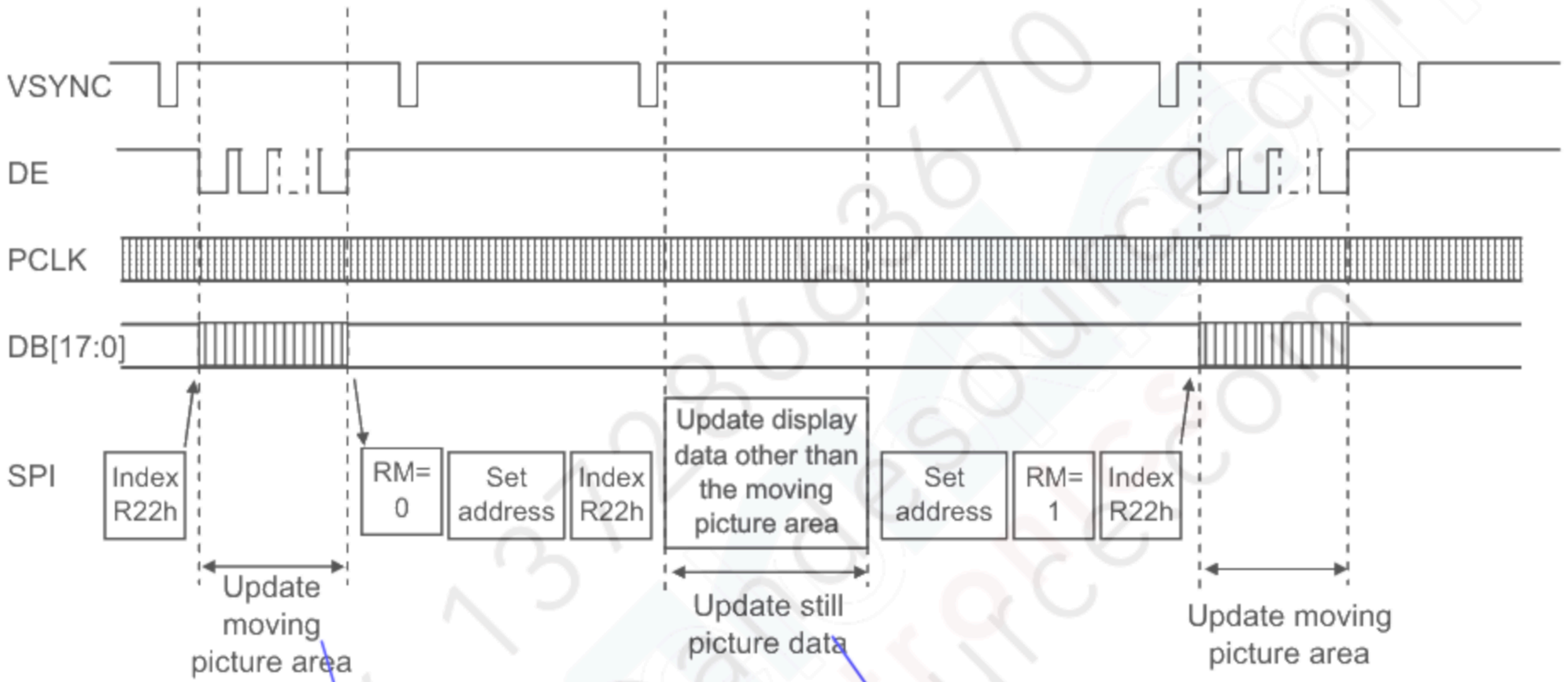
[RGB-I/F mode -> internal clock mode]



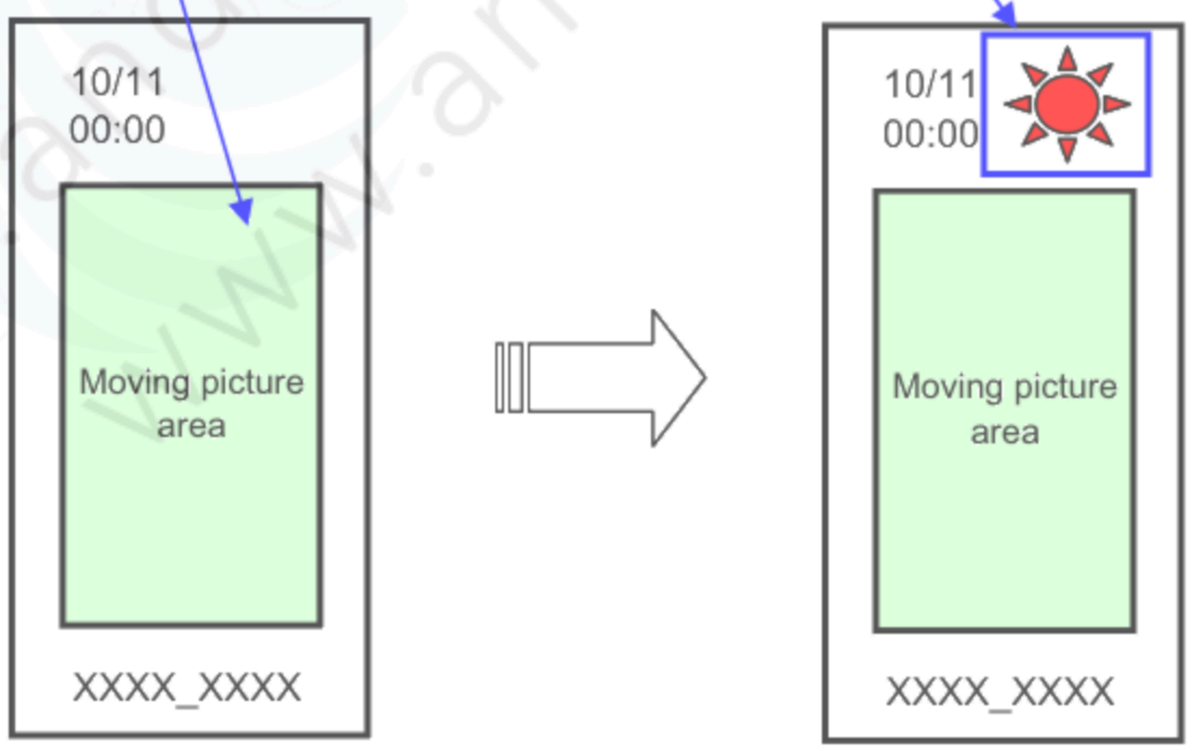
10.4 Update Still Picture Area in Moving Picture Mode

The panel allows GRAM access via the system interface (SPI) in RGB-I/F mode.
In RGB-I/F mode, the data are written to GRAM in synchronization with PCLK at DE=Low (DPL=0).
So, when write data to GRAM by system interface (SPI), set DE=Hi to terminate writing data by RGB-I/F.
And, set RM=0 to access GRAM by system interface (SPI).
When restart GRAM access in RGB-I/F mode, wait read/write cycle
and then set RM=1 and the INDEX register to R22h to start accessing GRAM via RGB-I/F.

Example of update the still picture data in moving picture mode.



Note1: Input VSYNC/HSYNC/PCLK constantly in RGB-I/F mode.
Note2: The address is set every falling edge of VSYNC (VSPL=0) in RGB-I/F mode.
Note3: Set address and INDEX register (R22h) before starting GRAM access
in RGB-I/F mode.
Note4: "Set address" is consist of setting window address and writing start address.



11. Sequence

11.1 Power-ON Sequence

Register	Data	Comment	Detail
VCC_ON		Power ON	
RESB = Low		Set RESB=0	
Wait ≧ 1 msec		Wait	
RESB = High		Set RESB=1	
Wait ≧ 50 msec		Wait	
R07h	0000h	Set R07h to turn off the panel.	DTE=0, D[1:0]=00, GON=0

LCD_Power Supply ON sequence

R10h	0000h	Initialize Power Control 1 (Stop operation)	SAP=0,BT[2:0]=3'b000,APE=0,AP[2:0]=3'b000, SLP=0,STB=0
R11h	0007h	Initialize Power Control 2 (Stop step-up)	DC1[2:0]=3'b000,DC0[2:0] =3'b000,VC[2:0] =3'b111
R12h	0000h	Initialize Power Control 3 (stop regulator)	VCIRE=0,VRH[3:0]=4'b0000
R13h	0000h	Initialize Vcom amplitude	VDV[4:0]= 5'b00000
Wait > 200 msec			
R10h	1390h	Set Amp / VGH･VGL	SAP=1,BT[2:0]=3'b011,APE=1,AP[2:0]=3'b001, SLP=0,STB=0
R11h	0113h	Set Step-up circuit operation	DC1[2:0]=3'b001,DC0[2:0]=3'b001,VC[2:0]=3'b011
Wait > 50 msec			
R12h	008Bh	Set Regulator circuit operation (Vreg1out=4.375V)	VCIRE=1,VRH[3:0]=4'b1011
Wait > 50 msec			
R13h	1500h	Set Vcom amplitude (Vcompp=4.55V)	VDV[4:0]= 5'b10101
RA2h	0001h	OTP Vcom_DC data enable	VCM_EN = 1
REFh	0211h	Set test register	
Wait > 50 msec			

Display setting

R01h	0400h	Source direction / Gate arrangement	SM=1, SS=0
R02h	0200h	Set line inversion	B/C=1
R03h	1030h	Set writing mode to GRAM	TRI=0,DFM=0,BGR=1,AM=0 (H direction), I/D=11(H:increment, V:increment)
R08h	****h	Set blank period	FP[7:0]=8'h**, BP[7:0]=8'h** (Note)
R0Ch	0001h	Set interface mode	ENC[2:0]=000, RM=0, DM[1:0]=00, RIM[1:0]=01
R0Fh	0000h	Set polarity of VSYNC/HSYNC/DE/PCLK	VSPL=0,HSPL=0,EPL=0, DPL=0
R2Bh	000Ah	Set frame rate	FRS[3:0]=4'b1010

Note: Set optimum value with reference to explanation on page 33.

Gamma setting

R30h	0303h	Set Gamma-fine for positive polarity	KP1[2:0]=3'h03	KP0[2:0]=3'h03
R31h	0304h	Set Gamma-fine for positive polarity	KP3[2:0]=3'h03	KP2[2:0]=3'h04
R32h	0303h	Set Gamma-fine for positive polarity	KP5[2:0]=3'h03	KP4[2:0]=3'h03
R35h	0104h	Set Gamma-gradient for positive polarity	RP1[2:0]=3'h01	RP0[2:0]=3'h04
R36h	0F0Bh	Set Gamma-amplitude for positive polarity	VRP1[4:0]=5'h0F	VRP0[3:0]=4'h0B
R37h	0404h	Set Gamma-fine for negative polarity	KN1[2:0]=3'h04	KN0[2:0]=3'h04
R38h	0304h	Set Gamma-fine for negative polarity	KN3[2:0]=3'h03	KN2[2:0]=3'h04
R39h	0304h	Set Gamma-fine for negative polarity	KN5[2:0]=3'h03	KN4[2:0]=3'h04
R3Ch	0202h	Set Gamma-gradient for negative polarity	RN1[2:0]=3'h02	RN0[2:0]=3'h02
R3Dh	0208h	Set Gamma-amplitude for negative polarity	VRN1[4:0]=5'h02	VRN0[3:0]=4'h08

(to next page)

(from previous page)

↓

RAM_address & Display setting

Register	Data	Comment	Detail
R50h	003Ch	Set Window_H start address	HSA[7:0]=8'h3C
R51h	00B3h	Set Window_H end address	HEA[7:0]=8'hB3
R52h	0000h	Set Window_V start address	VSA[8:0]=9'h000
R53h	013Fh	Set Window_V end address	VEA[8:0]=9'h13F
R60h	A700h	gate direction / position / number of line	GS=1, NL[5:0]=6'h27, SCN[5:0]=6'h00
R61h	0005h	Set output polarity	NDL=1, VLE=0, REV=1
R6Ah	0000h	Set scrolling amount	VL[8:0]=9'h000
R90h	0014h	Set 1 line clock number	DIVI[1:0]=2'b00,RTNI[4:0]=10100(20clk,60Hz)
R92h	0600h	Set gate output timing	NOWI[2:0] = 3'h6
R95h	0200h	Set gate output timing in RGB-I/F mode	DIVE[1:0]=2'b10 (1/8)
R97h	0700h	Set gate output timing in RGB-I/F mode	NOWE[3:0] = 4'h7 (8clk x 7=56clk)

↓

Display_ON sequence

R07h	0001h	Connect gate to VGH, source to GND	GON=0,DTE=0,D[1:0]=01
Wait > 35 msec			
R07h	0021h	Connect gate to VGL, source to GND	GON=1,DTE=0,D[1:0]=01
R07h	0123h	Connect gate to VGL, source to normal	GON=1,DTE=0,D[1:0]=11
Wait > 35 msec			
R07h	0133h	Connect gate and source to normal	GON=1,DTE=1,D[1:0]=11,BASEE=1

↓

RAM_address setting

R20h	003Ch	Set start address to write to GRAM	AD[7:0]=8'h3C
R21h	0000h	Set start address to write to GRAM	AD[16:8]=9'h000
R0Ch	0111h	Set RGB-I/F mode	ENC[2:0]=000, RM=1, DM[1:0]=01, RIM[1:0]=01
R22h		Set start index to write to GRAM	

11.2 Power-OFF / Standby Sequence

Display_OFF sequence

Register	Data	Comment	Detail
R07h	0131h	Connect source to GND	GON=1,DTE=1,D[1:0]=01,BASEE=1
Wait > 35 msec			
R07h	0130h	Stop internal operation	GON=1,DTE=1,D[1:0]=00,BASEE=1
Wait > 35 msec			
R07h	0000h	Display OFF	GON=0,DTE=0,D[1:0]=00,BASEE=0

↓

Standby setting

R10h	0001h	Set standby mode	SAP=0,BT[2:0]=3'b000,APE=0,AP[2:0]=3'b000, SLP=0,STB=1

↓

Power-OFF

VCC_OFF	Power OFF	

11.3 Standby Release Sequence

Standby cancel

Register	Data	Comment	Detail
R10h	0000h	standby cancel	STB=0
R10h	0190h	Set step-up circuit, start operation	BT[2:0]=3'b001,APE=1,AP[2:0]=3'b001
Wait > 80 msec			
R07h	0000h	Display OFF	DTE=0, D[1:0]=00, GON=0

↓

LCD_Power Supply ON sequence

R10h	0000h	Initialize Power Control 1 (Stop operation)	SAP=0,BT[2:0]=3'b000,APE=0,AP[2:0]=3'b000, SLP=0,STB=0
R11h	0007h	Initialize Power Control 2 (Stop step-up)	DC1[2:0]=3'b000,DC0[2:0] =3'b000,VC[2:0] =3'b111
R12h	0000h	Initialize Power Control 3 (stop regulator)	VCIRE=0,VRH[3:0]=4'b0000
R13h	0000h	Initialize Vcom amplitude	VDV[4:0]= 5'b00000
Wait > 200 msec			
R10h	1390h	Set Amp / VGH･VGL	SAP=1,BT[2:0]=3'b011,APE=1,AP[2:0]=3'b001, SLP=0,STB=0
R11h	0113h	Set Step-up circuit operation	DC1[2:0]=3'b001,DC0[2:0]=3'b001,VC[2:0]=3'b011
Wait > 50 msec			
R12h	008Bh	Set Regulator circuit operation (Vreg1out=4.375V)	VCIRE=1,VRH[3:0]=4'b1011
Wait > 50 msec			
R13h	1500h	Set Vcom amplitude (Vcompp=4.55V)	VDV[4:0]= 5'b10101
RA2h	0001h	OTP Vcom_DC data enable	VCM_EN = 1
REFh	0211h	Set test register	
Wait > 50 msec			

↓

Display setting

R01h	0400h	Source direction / Gate arrangement	SM=1, SS=0
R02h	0200h	Set line inversion	B/C=1
R03h	1030h	Set writing mode to GRAM	TRI=0,DFM=0,BGR=1,AM=0 (H direction), I/D=11(H:increment, V:increment)
R08h	****h	Set blank period	FP[7:0]=8'h**, BP[7:0]=8'h** (Note)
R0Ch	0001h	Set interface mode	ENC[2:0]=000, RM=0, DM[1:0]=00, RIM[1:0]=01
R0Fh	0000h	Set polarity of VSYNC/HSYNC/DE/PCLK	VSPL=0,HSPL=0,EPL=0, DPL=0
R2Bh	000Ah	Set frame rate	FRS[3:0]=4'b1010

Note: Set optimum value with reference to explanation on page 33.

↓

(to next page)

(from previous page)

Gamma setting

Register	Data	Comment	Detail	
R30h	0303h	Set Gamma-fine for positive polarity	KP1[2:0]=3'h03	KP0[2:0]=3'h03
R31h	0304h	Set Gamma-fine for positive polarity	KP3[2:0]=3'h03	KP2[2:0]=3'h04
R32h	0303h	Set Gamma-fine for positive polarity	KP5[2:0]=3'h03	KP4[2:0]=3'h03
R35h	0104h	Set Gamma-gradient for positive polarity	RP1[2:0]=3'h01	RP0[2:0]=3'h04
R36h	0F0Bh	Set Gamma-amplitude for positive polarity	VRP1[4:0]=5'h0F	VRP0[3:0]=4'h0B
R37h	0404h	Set Gamma-fine for negative polarity	KN1[2:0]=3'h04	KN0[2:0]=3'h04
R38h	0304h	Set Gamma-fine for negative polarity	KN3[2:0]=3'h03	KN2[2:0]=3'h04
R39h	0304h	Set Gamma-fine for negative polarity	KN5[2:0]=3'h03	KN4[2:0]=3'h04
R3Ch	0202h	Set Gamma-gradient for negative polarity	RN1[2:0]=3'h02	RN0[2:0]=3'h02
R3Dh	0208h	Set Gamma-amplitude for negative polarity	VRN1[4:0]=5'h02	VRN0[3:0]=4'h08

RAM_address & Display setting

R50h	003Ch	Set Window_H start address	HSA[7:0]=8'h3C
R51h	00B3h	Set Window_H end address	HEA[7:0]=8'hB3
R52h	0000h	Set Window_V start address	VSA[8:0]=9'h000
R53h	013Fh	Set Window_V end address	VEA[8:0]=9'h13F
R60h	A700h	gate direction / position / number of line	GS=1, NL[5:0]=6'h27, SCN[5:0]=6'h00
R61h	0005h	Set output polarity	NDL=1, VLE=0, REV=1
R6Ah	0000h	Set scrolling amount	VL[8:0]=9'h000
R90h	0014h	Set 1 line clock number	DIVI[1:0]=2'b00,RTNI[4:0]=10100(20clk,60Hz)
R92h	0600h	Set gate output timing	NOWI[2:0] = 3'h6
R95h	0200h	Set gate output timing in RGB-I/F mode	DIVE[1:0]=2'b10 (1/8)
R97h	0700h	Set gate output timing in RGB-I/F mode	NOWE[3:0] = 4'h7 (8clk x 7=56clk)

Display_ON sequence

R07h	0001h	Connect gate to VGH, source to GND	GON=0,DTE=0,D[1:0]=01
Wait > 35 msec			
R07h	0021h	Connect gate to VGL, source to GND	GON=1,DTE=0,D[1:0]=01
R07h	0123h	Connect gate to VGL, source to normal	GON=1,DTE=0,D[1:0]=11
Wait > 35 msec			
R07h	0133h	Connect gate and source to normal	GON=1,DTE=1,D[1:0]=11,BASEE=1

RAM_address setting

R20h	003Ch	Set start address to write to GRAM	AD[7:0]=8'h3C
R21h	0000h	Set start address to write to GRAM	AD[16:8]=9'h000
R0Ch	0111h	Set RGB-I/F mode	ENC[2:0]=000, RM=1, DM[1:0]=01, RIM[1:0]=01
R22h		Set start index to write to GRAM	

11.4 Refresh Sequence 1

To prevent false operation by static electricity and such, please refresh register setting as follows regularly.

Power_up sequence

Register	Data	Comment	Detail
R10h	1390h	Set Amp / VGH･VGL	SAP=1,BT[2:0]=3'b011,APE=1,AP[2:0]=3'b001, SLP=0,STB=0
R11h	0113h	Set Step-up circuit operation	DC1[2:0]=3'b001,DC0[2:0]=3'b001,VC[2:0]=3'b011
R12h	008Bh	Set Regulator circuit operation (Vreg1out=4.375V)	VCIRE=1,VRH[3:0]=4'b1011
R13h	1500h	Set Vcom amplitude (Vcompp=4.55V)	VDV[4:0]= 5'b10101
RA2h	0001h	OTP Vcom_DC data enable	VCM_EN = 1

Display setting

R01h	0400h	Source direction / Gate arrangement	SM=1, SS=0
R02h	0200h	Set line inversion	B/C=1
R03h	1030h	Set writing mode to GRAM	TRI=0,DFM=0,BGR=1,AM=0 (H direction), I/D=11(H:increment, V:increment)
R08h	****h	Set blank period	FP[7:0]=8'h**, BP[7:0]=8'h** (Note)
R0Fh	0000h	Set polarity of VSYNC/HSYNC/DE/PCLK	VSPL=0,HSPL=0,EPL=0, DPL=0
R2Bh	000Ah	Set frame rate	FRS[3:0]=4'b1010

Note: Set optimum value with reference to explanation on page 33.

Gamma setting

R30h	0303h	Set Gamma-fine for positive polarity	KP1[2:0]=3'h03 KP0[2:0]=3'h03
R31h	0304h	Set Gamma-fine for positive polarity	KP3[2:0]=3'h03 KP2[2:0]=3'h04
R32h	0303h	Set Gamma-fine for positive polarity	KP5[2:0]=3'h03 KP4[2:0]=3'h03
R35h	0104h	Set Gamma-gradient for positive polarity	RP1[2:0]=3'h01 RP0[2:0]=3'h04
R36h	0F0Bh	Set Gamma-amplitude for positive polarity	VRP1[4:0]=5'h0F VRP0[3:0]=4'h0B
R37h	0404h	Set Gamma-fine for negative polarity	KN1[2:0]=3'h04 KN0[2:0]=3'h04
R38h	0304h	Set Gamma-fine for negative polarity	KN3[2:0]=3'h03 KN2[2:0]=3'h04
R39h	0304h	Set Gamma-fine for negative polarity	KN5[2:0]=3'h03 KN4[2:0]=3'h04
R3Ch	0202h	Set Gamma-gradient for negative polarity	RN1[2:0]=3'h02 RN0[2:0]=3'h02
R3Dh	0208h	Set Gamma-amplitude for negative polarity	VRN1[4:0]=5'h02 VRN0[3:0]=4'h08

RAM_address & Display setting

R50h	003Ch	Set Window_H start address	HSA[7:0]=8'h3C
R51h	00B3h	Set Window_H end address	HEA[7:0]=8'hB3
R52h	0000h	Set Window_V start address	VSA[8:0]=9'h000
R53h	013Fh	Set Window_V end address	VEA[8:0]=9'h13F
R60h	A700h	gate direction / position / number of line	GS=1, NL[5:0]=6'h27, SCN[5:0]=6'h00
R61h	0005h	Set output polarity	NDL=1, VLE=0, REV=1
R6Ah	0000h	Set scrolling amount	VL[8:0]=9'h000
R90h	0014h	Set 1 line clock number	DIVI[1:0]=2'b00,RTNI[4:0]=10100(20clk,60Hz)
R92h	0600h	Set gate output timing	NOWI[2:0] = 3'h6
R95h	0200h	Set gate output timing in RGB-I/F mode	DIVE[1:0]=2'b10 (1/8)
R97h	0700h	Set gate output timing in RGB-I/F mode	NOWE[3:0] = 4'h7 (8clk x 7=56clk)

Display_ON sequence

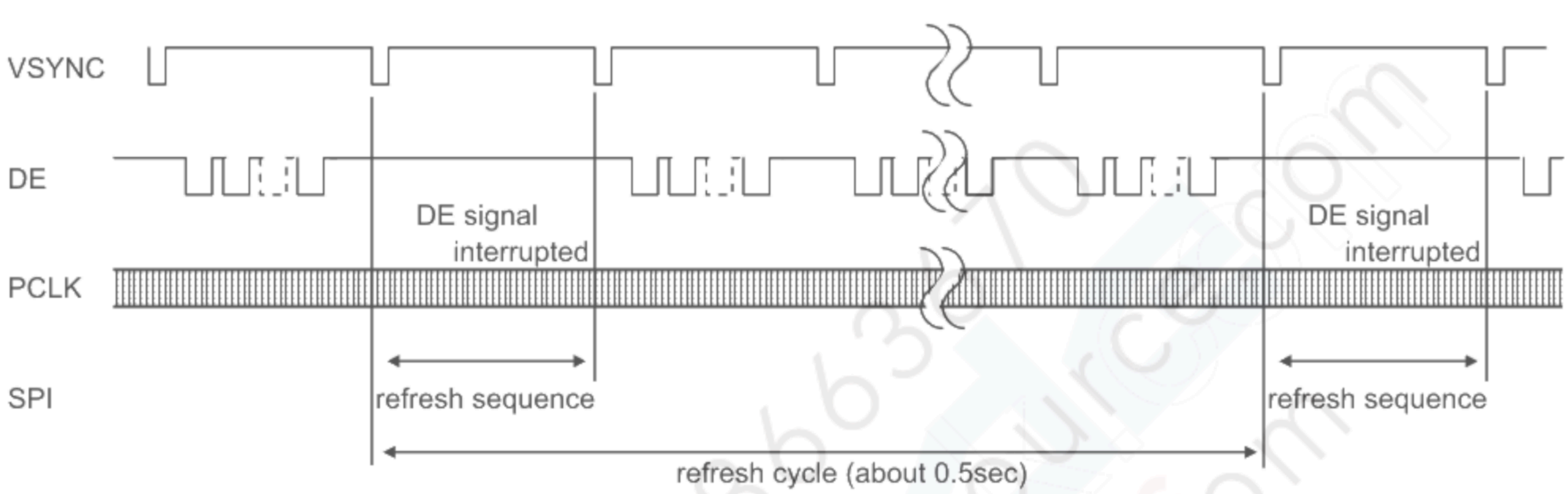
R07h	0133h	Connect gate and source to normal	GON=1,DTE=1,D[1:0]=11,BASEE=1

RAM_address setting

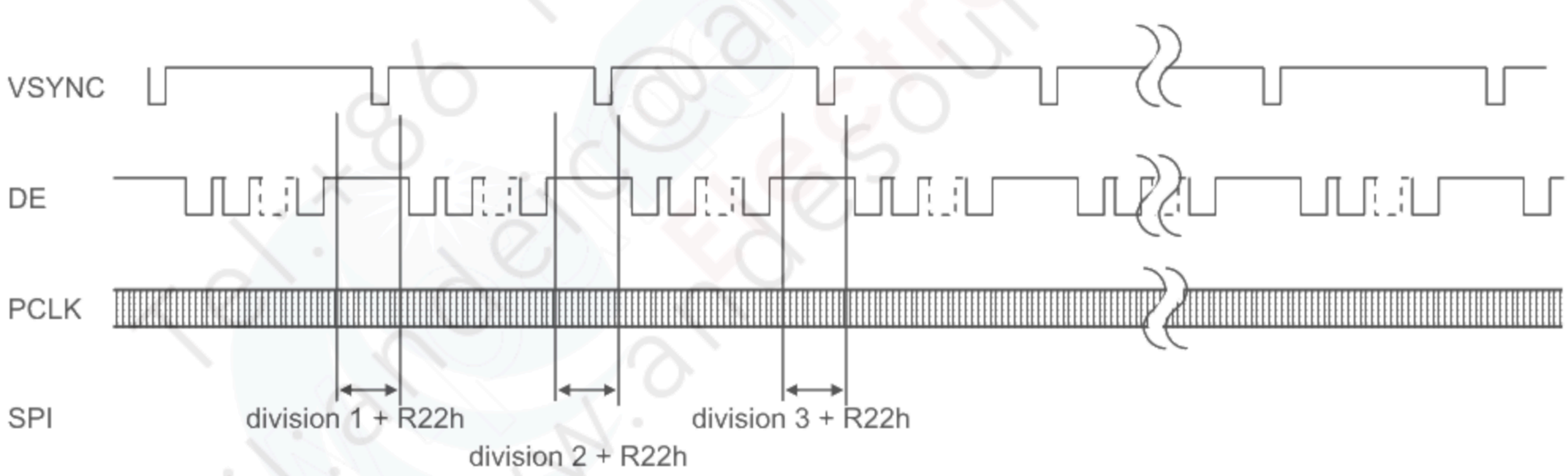
R20h	003Ch	Set start address to write to GRAM	AD[7:0]=8'h3C
R21h	0000h	Set start address to write to GRAM	AD[16:8]=9'h000
R0Ch	0111h	Set RGB-I/F mode	ENC[2:0]=000, RM=1, DM[1:0]=01, RIM[1:0]=01
R22h		Set start index to write to GRAM	

This panel write display data to GRAM only when the INDEX register R22h is set.
Please execute the refresh sequence 1 with in one of two ways as follows.

1) Execute the refresh sequence during 1V period with DE=Hi (non-active).

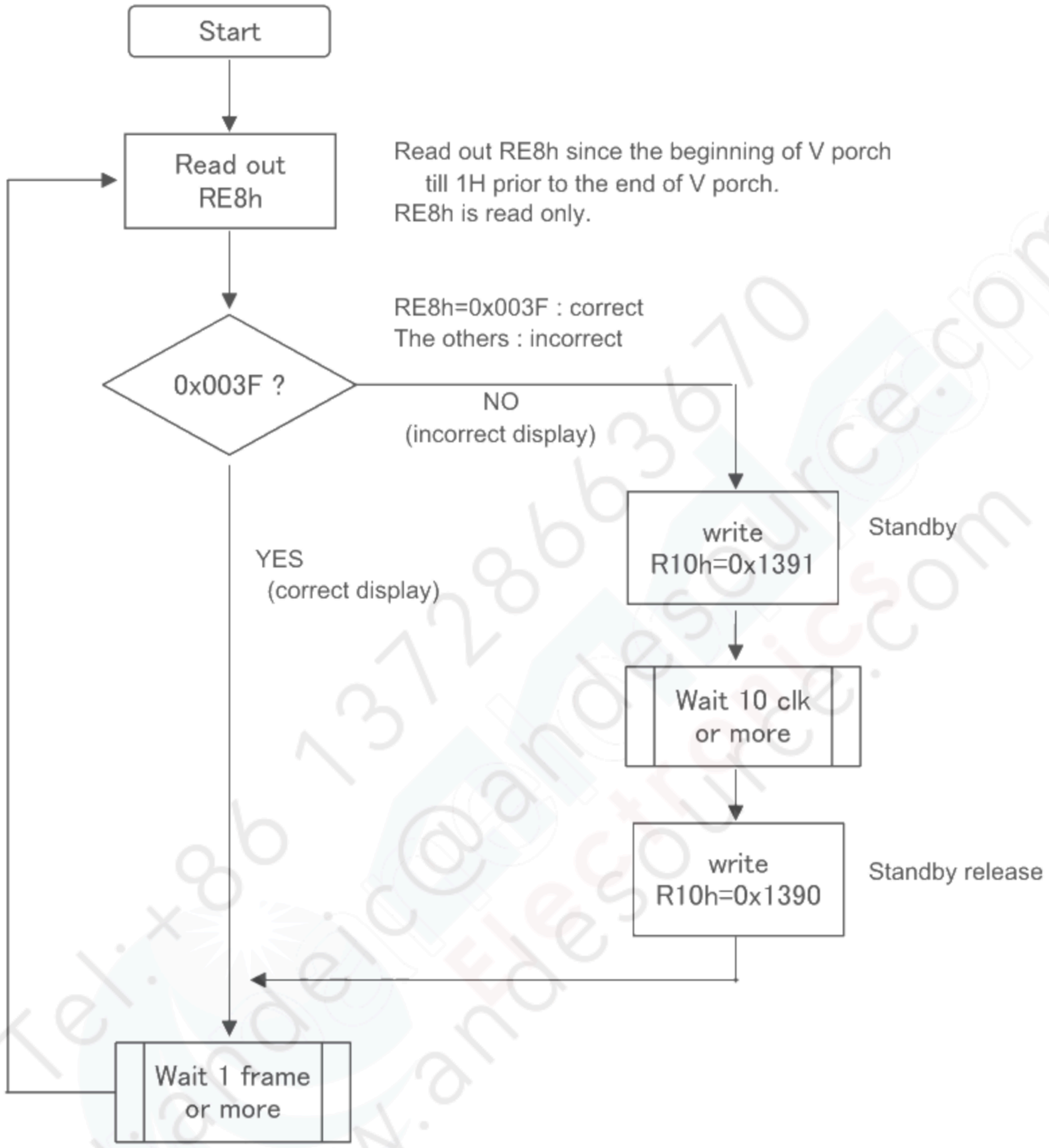


2) Execute the refresh sequence that are divided during V porch period in order,
and transfer R22h at the last of each divided sequence block.



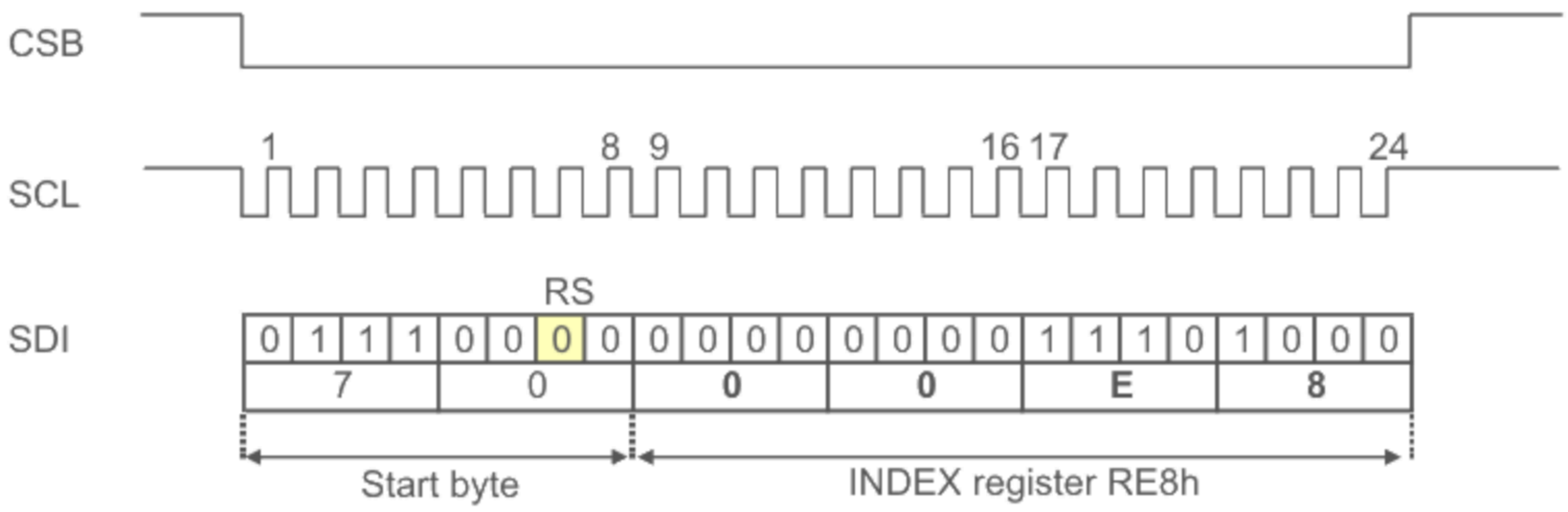
11.5 Refresh Sequence 2

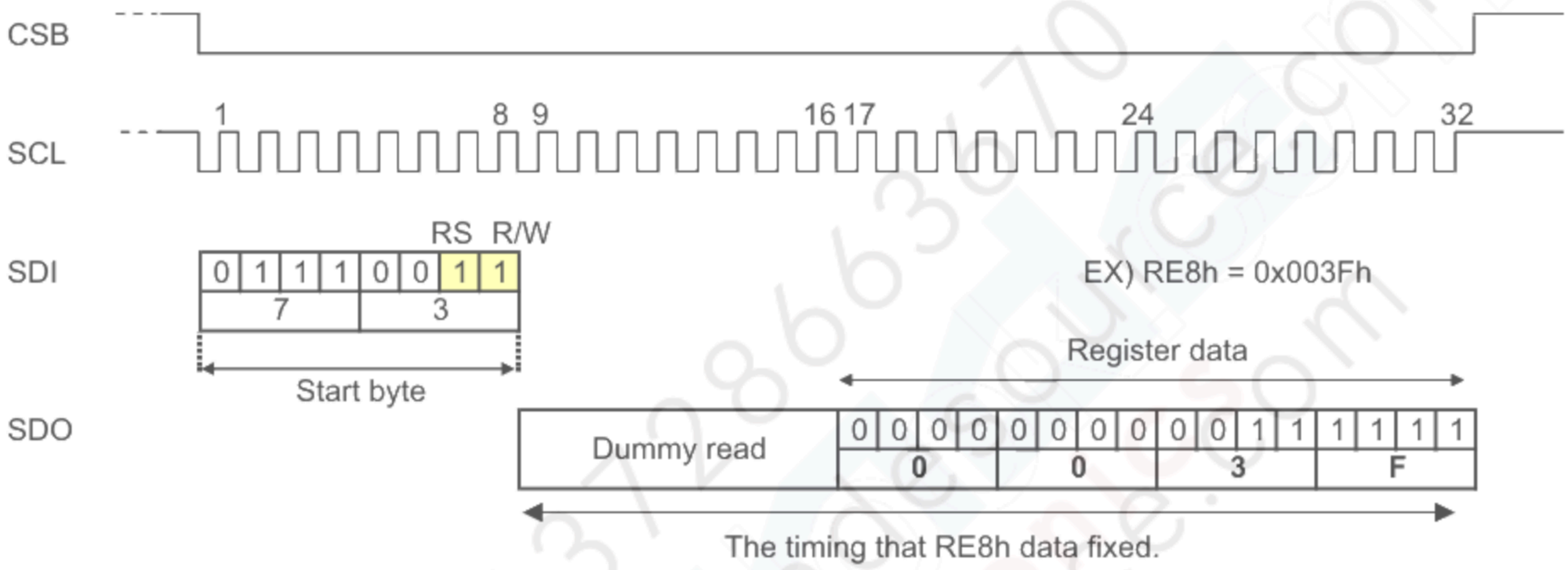
When incorrect display occurred, that was not able to return to correct display by refresh sequence 1, by static electricity and such, read out the register and execute refresh sequence 2 as follows.
Please read out and check this register regularly.



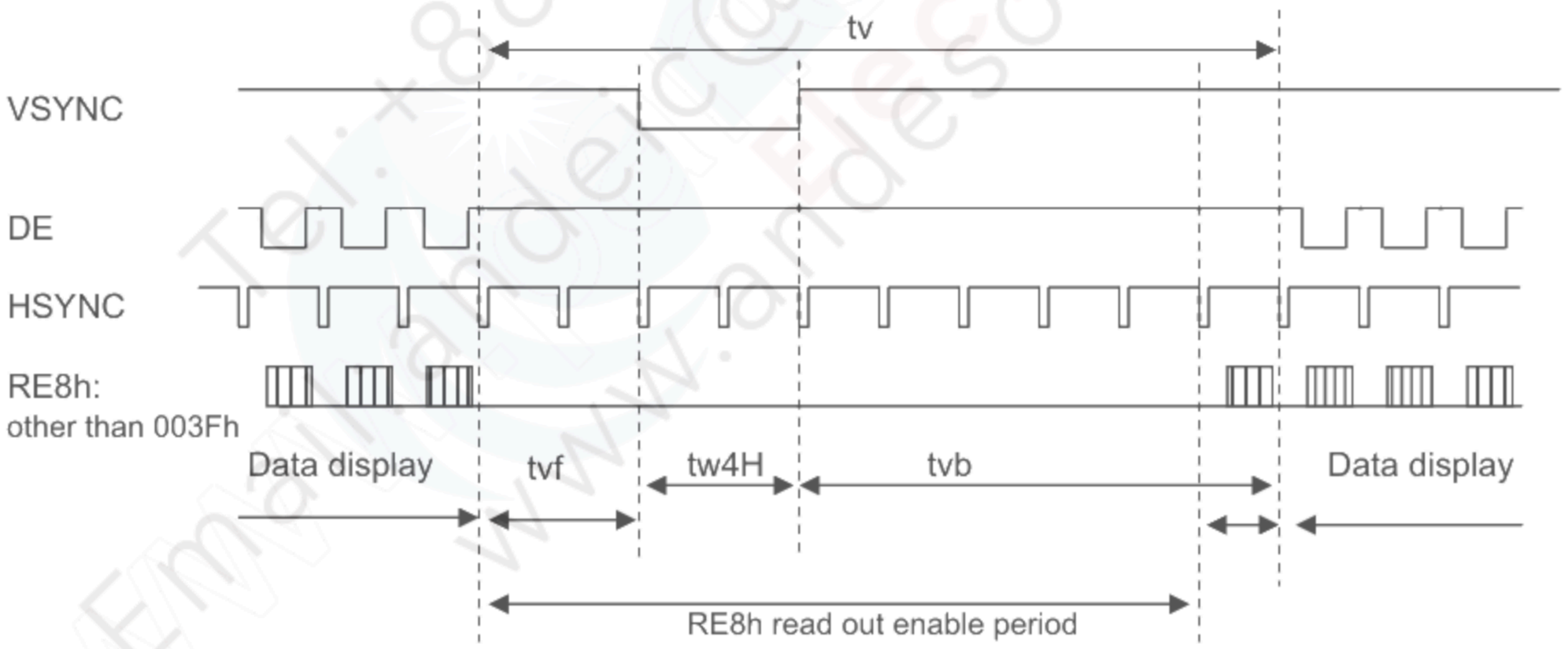
RE8h outputs 003Fh at correct display, but the other values at incorrect display.
To set "standby" and "standby release" return from incorrect display to correct display.
Therefore, if the output value of RE8h is not 003Fh, set "standby" and "standby release" with R10h.

The configuration of register read out is shown below.
EX: RE8h = 0x003Fh





The timing that RE8h data fixed is shown above.
It is possible to detect incorrect display by reading out RE8h during the period shown below.



Read out RE8h since the end of data display period (beginning of V porch)
till 1H prior to the beginning of next data display period.

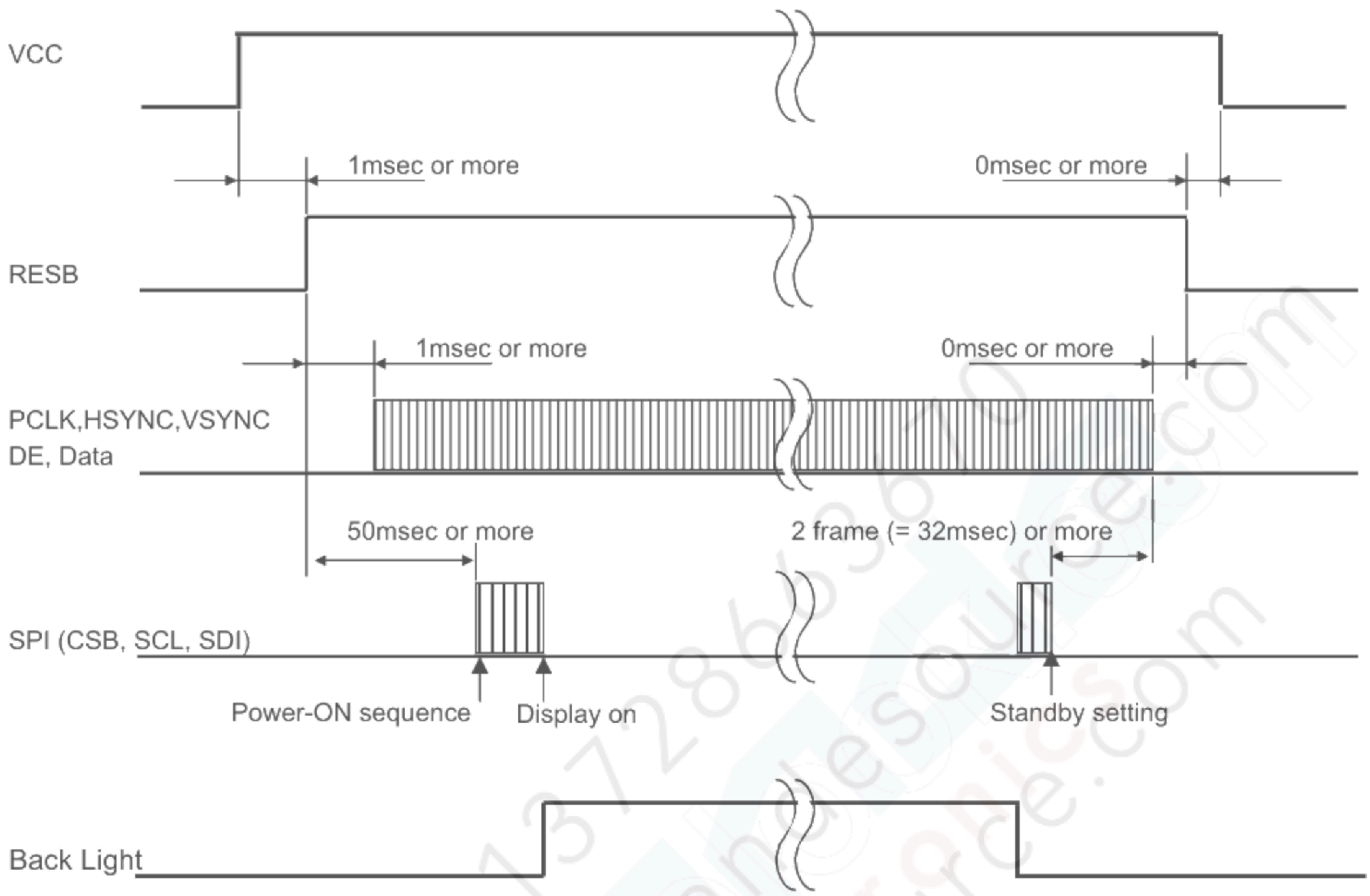
The optimum value that set to R08h is depend on tvf and tw4H + tvb setting values.
(Refer to Register List on page 19.)

FP=tvf
BP=tw4H+tvb

Note) tvf>=2H, tw4H>=1H, tvb>=2H, 5H<=(tvf+tw4H+tvb)<=30H

The value of RE8h starts to change since 1H prior to setting value of BP.

11.6 Power-ON / Power-OFF Diagram



12. Characteristics

12.1 Optical Characteristics

< Measurement Condition >

Measuring instruments: CS1000（KONICA MINOLTA）, LCD7000(OTSUKA ELECTRONICS）, EZcontrast160D（ELDIM）

Driving condition: VCC=3.3V,VSS=0V
Optimized VCOMDC

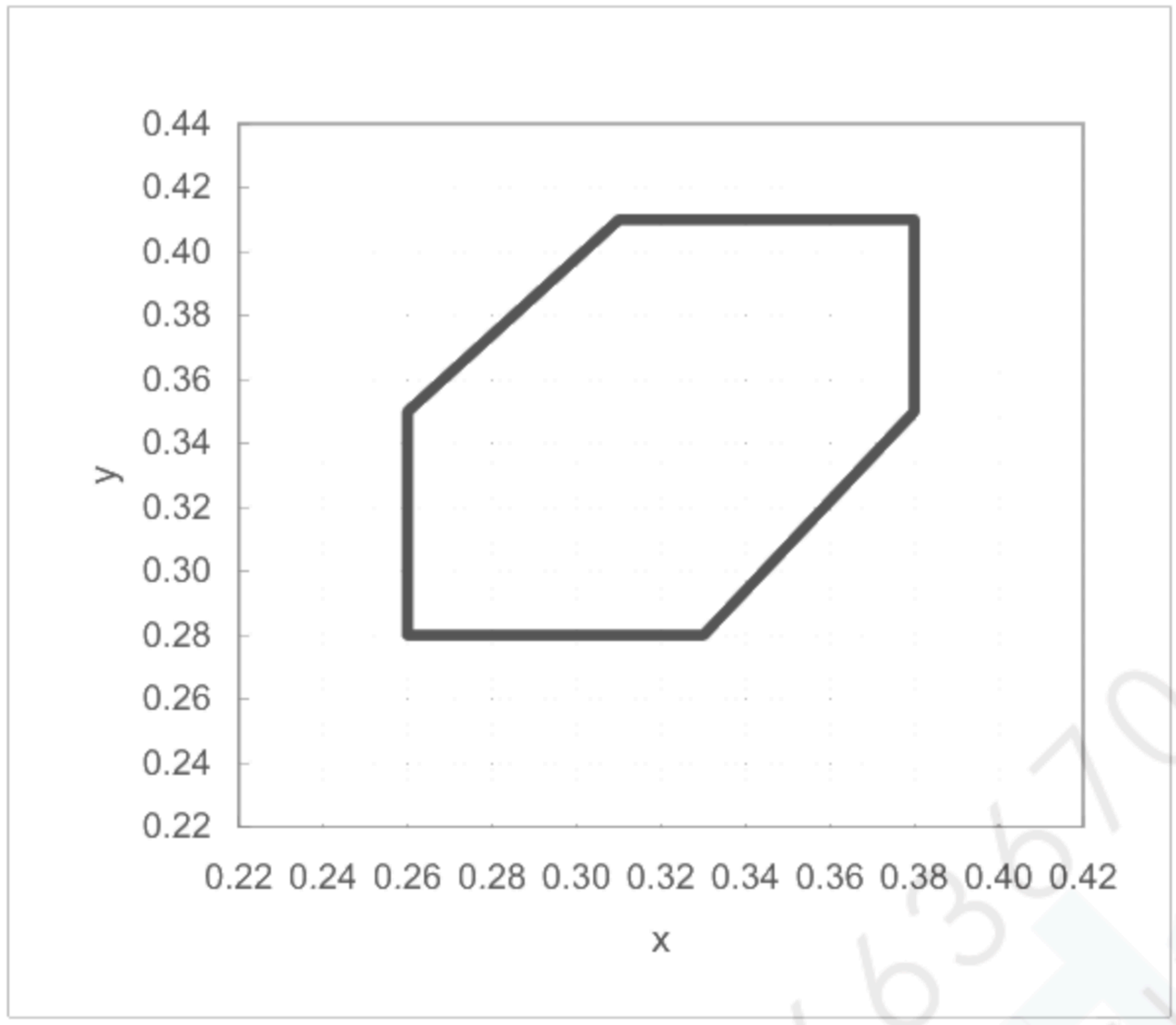
Backlight: IL= 35.0 mA

Measured temperature: Ta=25° C

Item		Symbol	Condition	MIN	TYP	MAX	Unit	Note No.	Remark
Response time	Rise time	TON	[Data]= 3Fh→00h	—	—	40	ms	1	※
	Fall time	TOFF	[Data]= 00h→3Fh	—	—	60	ms		
Contrast ratio		CR	[Data]= 3Fh/00h	—	300	—		2	
Viewing angle	Left	θL	[Data]= 3Fh/00h CR≧5	—	80	—	deg	3	※
	Right	θR		—	80	—	deg		
	Up	φU		—	80	—	deg		
	Down	φD		—	80	—	deg		
White Chromaticity		x	[Data]=3Fh	White chromaticity range				4	
		y							
Burn-in				No noticeable burn-in image should be observed after 2 hours of window pattern display.				5	
Center brightness			[Data]=3Fh	375	625	—	cd/m^2	6	
Brightness distribution			[Data]=3Fh	70	—	—	%	7	

* Note number 1 to 7: Refer to the APPENDIX of "Reference Method for Measuring Optical Characteristics".

※ Measured in the form of LCD module.



White Chromaticity Range

【White Chromaticity Range】

x	y
0.31	0.41
0.26	0.35
0.26	0.28
0.33	0.28
0.38	0.35
0.38	0.41

12.2 Temperature Characteristics

< Measurement Condition >

Measuring instruments: CS1000 (KONICA MINOLTA), LCD7000(OTSUKA ELECTRONICS)

Driving condition: VCC=3.3V,VSS=0V
Optimized VCOMDC

Backlight: IL= 35.0 mA

Item			Specification		Remark
			Ta＝－10° C	Ta＝70° C	
Contrast ratio		CR	40 or more	40 or more	
Response time	Rise time	TON	200 msec or less	30 msec or less	※
	Fall time	TOFF	300 msec or less	50 msec or less	※
Display Quality			No noticeable display defect or ununiformity should be observed.		Use the criteria for judgment specified in the section 13.

※ Measured in the form of LCD module.

13. Criteria of Judgment

13.1 Defective Display and Screen Quality

Test Condition:	Observed TFT-LCD monitor from front during operation with the following conditions
Driving Signal	Raster Patter (white, RGB in monochrome, black)
Signal condition	[Data]:3Fh, 20h, 00h (3steps)
Observation distance	30 cm
Illuminance	200 to 350 lx
Backlight	IL= 35.0 mA

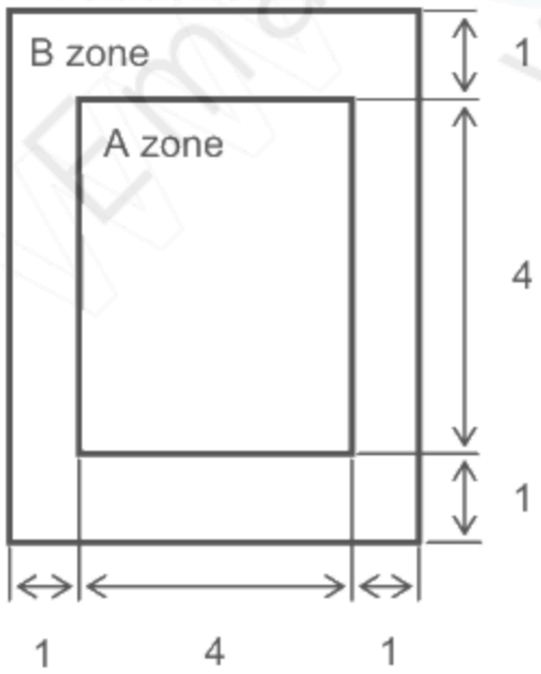
Defect item		Defect content		Criteria
Display Quality	Line defect	Black, white or color line, 3 or more neighboring defective dots		Not exists
	Dot defect	Uneven brightness on dot-by-dot base due to defective TFT or CF, or dust is counted as dot defect (brighter dot, darker dot) High bright dot: Visible through 2% ND filter at [Data]=00h Low bright dot: Visible through 5% ND filter at [Data]=00h Dark dot: Appear dark through white display at [Data]=20h		Refer to table 1
Screen Quality	Dirt	Point-like uneven brightness (white stain, black stain etc)		Invisible through 1% ND filter
	Foreign particle	Point-like	0.25mm<φ	N=0
			0.20<φ≦0.25mm	N≦2
			φ≦0.20mm	Ignored
		Liner	3.0mm<length and 0.08mm<width	N=0
			length≦3.0mm or width≦0.08mm	Ignored
	Others			Use boundary sample for judgment when necessary

φ(mm): Average diameter = (major axis + minor axis)/2
Permissible number: N

Table 1

Area	High bright dot	Low bright dot	Dark dot	Total	Criteria
A	0	2	2	3	Permissible distance between same color bright dots (includes neighboring dots): 3 mm or more
B	2	4	4	6	Permissible distance between same color high bright dots (includes neighboring dots): 5 mm or more
Total	2	4	4	6	

<Portrait model>



Division of A and B areas
B area: Active area
Dimensional ratio between A and B areas: 1: 4: 1 (Refer to the left figure)

13.2 Screen and Other Appearance

Testing conditions

Observation distance	30cm
Illuminance	1200～2000 lx

Item		Criteria	Remark
Polarizer	Flaw Stain Bubble Dust Dent	Ignore invisible defect when the backlight is on.	Applicable area: Active area only (Refer to the section 3.2 "Outward form")
S-case		No functional defect occurs	
FPC cable		No functional defect occurs	

14. Reliability Test

Test item		Test condition	number of failures /number of examinations
Durability test	High temperature storage	Ta=80°C 240H	0／3
	Low temperature storage	Ta=-30°C 240H	0／3
	High temperature & high humidity storage	Ta=60°C, RH=90% 240H non condensing ※	0／3
	High temperature operation	Tp=70°C 240H	0／3
	Low temperature operation	Tp=-20°C 240H	0／3
	High temp & humid operation	Tp=40°C, RH=90% 240H non condensing ※	0／3
	Thermal shock storage	-30←→80°C(30min/30min) 100 cycles	0／3
Mechanical environmental test	Electrostatic discharge test (Non operation)	Confirms to EIAJ ED-4701/300 C=200pF,R=0Ω,V=±200V Each 3 times of discharge on and power supply and other terminals.	0／3
	Surface discharge test (Non operation)	C=250pF, R=100Ω, V=±12kV Each 5 times of discharge in both polarities on the center of screen with the case grounded.	0／3
	Vibration test	Total amplitude 1.5mm, f=10～55Hz, X,Y,Z directions for each 2 hours	0／3
	Impact test	Use ORTUS TECHNOLOGY original jig (see next page)and make an impact with peak acceleration of 1000m/s2 for 6 msec with half sine-curve at 3 times to each X, Y, Z directions in conformance with JIS 60068-2-27-2011.	0／3
Packing test	Packing vibration-proof test	Acceleration of 19.6m/s^2 with frequency of 10→55→10Hz, X,Y, Zdirection for each 30 minutes	0／1 Packing
	Packing drop test	Drop from 75cm high. 1 time to each 6 surfaces, 3 edges, 1 corner	0／1 Packing

Note:Ta=ambient temperature Tp=Panel temperature

※ The profile of high temperature/humidity storage and High Temperature/humidity operation
(Pure water of over 10MΩ·cm shall be used.)

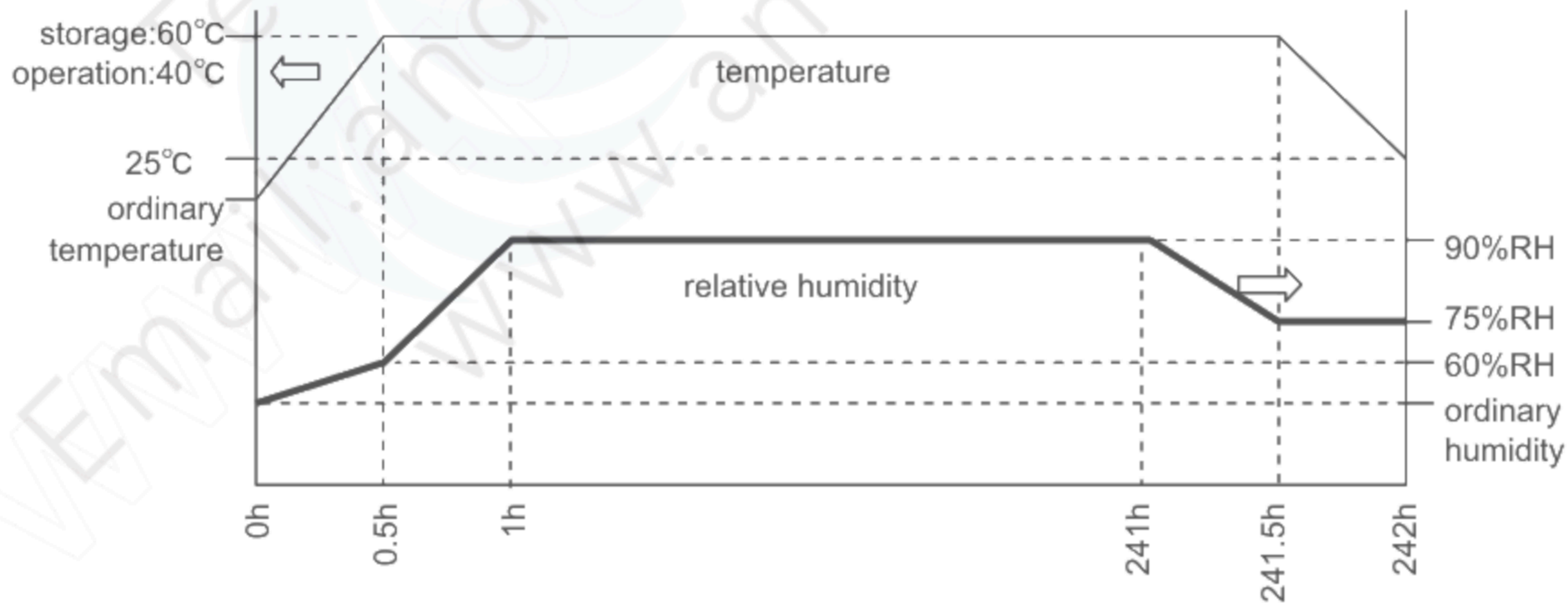
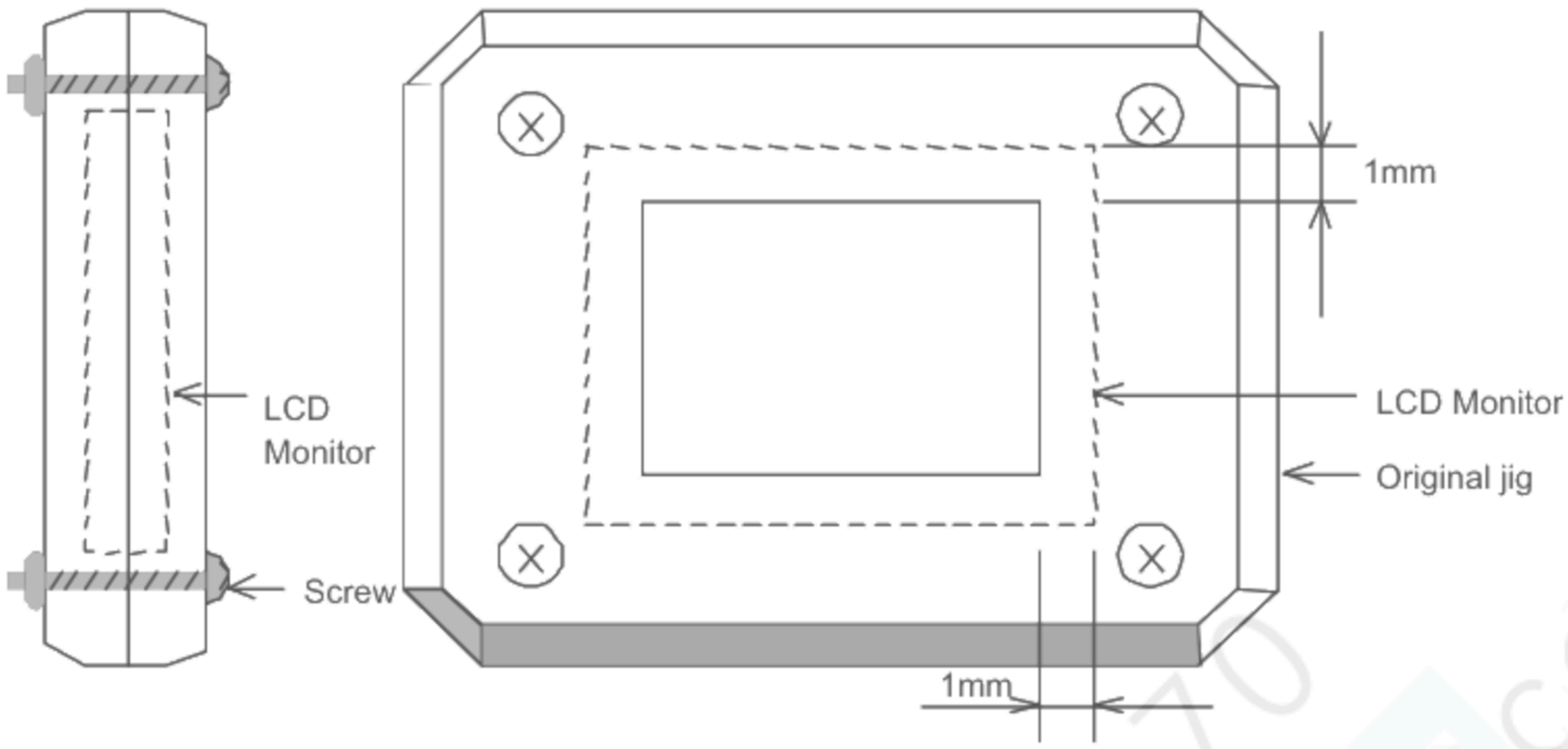


Table2.Reliability Criteria

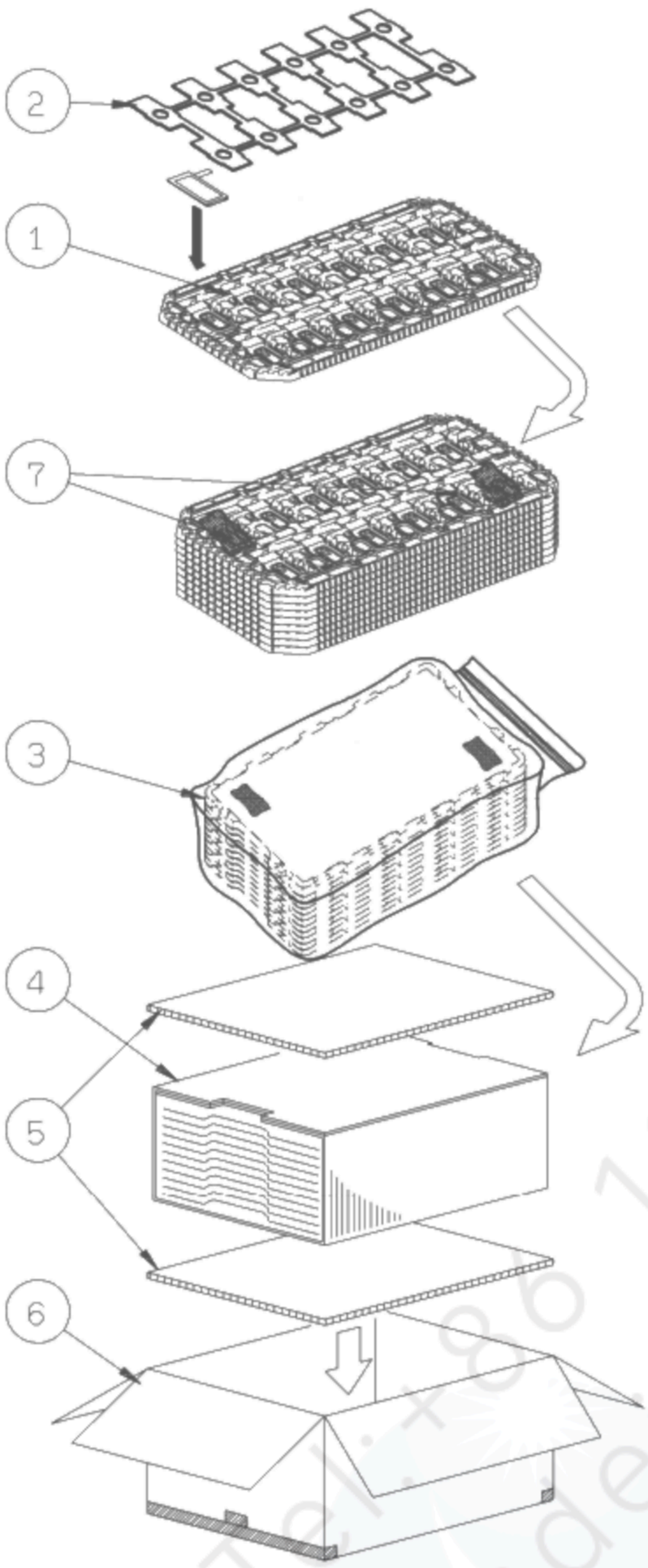
The parameters should be measured after leaving the monitor at the ordinary temperature for 24 hours or more after the test completion.

item	Standard	Remarks
Display quality	No visible abnormality shall be seen.	
Contrast ratio	40 or more	

ORTUS TECHNOLOGY Original Jig



15. Packing Specifications



Step 1. Each product is to be placed in one of the cut-outs of the tray
with the display surface facing upward. (12products per tray)
Foam sheet is to be placed on the products in the tray.

Step 2. Each tray is to be piled up in same orientation and the trays be in a stack of 8.
One empty tray is to be put on the top of stack of 8 trays.

Step 3. 2 packs of moisture absobers are to be placed on the top tray
as shown in the drawing.
Put piled trays into a sealing bag.
Vacuum and seal the sealing bag with the vacuum sealing machine.

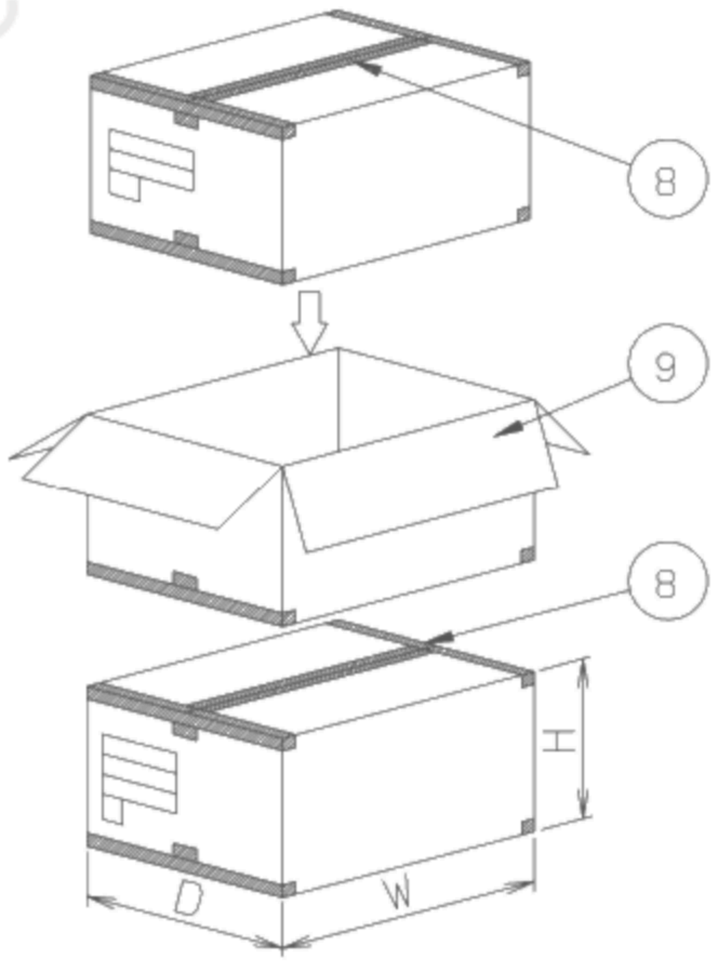
Step 4. The stack of trays in the plastic back is to be inserted into a inner carton.

Step 5. A corrugated board is to be placed on the top and on the bottom
of the inner carton.
The two corrugated boards and the inner carton is to be inserted into
an outer carton.

Step 6. The outer carton needs to sealed with packing tape
as shown in the drawing.
The model number, quantity of products, and shipping date are
to be printed on the outer carton.
If necessary, shipping labels or impression markings are
to be put on the outer carton.

Step 7. The outer carton is to be inserted into a extra outer carton with same direction.

Step 8. The extra outer carton needs to sealed with packing tape
as shown in the drawing.
The model number, quantity of products, and shipping date are
to be printed on the extra outer carton.
If necessary, shipping labels or impression markings are
to be put on the extra outer carton.



Remark: The return of packing materials is not required.

Packing item name		Specs., Material
①	Tray	A-PET
②	Antistatic foam sheet	Polyethylene foam
③	Sealing bag	
④	Inner carton	Corrugated cardboard
⑤	Inner board	Corrugated cardboard
⑥	Outer carton	Corrugated cardboard
⑦	Drier	Moisture absorber
⑧	Packing tape	
⑨	Extra outer carton	Corrugated cardboard

Dimension of extra outer carton	
D : Approx.	(338mm)
W : Approx.	(549mm)
H : Approx.	(198mm)
Quantity of products packed in one carton:	96
Gross weight : Approx.	6.3Kg

16. Handling Instruction

16.1 Cautions for Handling LCD panels

Caution

(1) Do not make an impact on the LCD panel glass because it may break and you may get injured from it.

(2) If the glass breaks, do not touch it with bare hands.
(Fragment of broken glass may stick you or you cut yourself on it.

(3) If you get injured, receive adequate first aid and consult a medial doctor.

(4) Do not let liquid crystal get into your mouth.
(If the LCD panel glass breaks, try not let liquid crystal get into your mouth even toxic property of liquid crystal has not been confirmed.

(5) If liquid crystal adheres, rinse it out thoroughly.
(If liquid crystal adheres to your cloth or skin, wipe it off with rubbing alcohol or wash it thoroughly with soap. If liquid crystal gets into eyes, rinse it with clean water for at least 15 minutes and consult an eye doctor.

(6) If you scrap this products, follow a disposal standard of industrial waste that is legally valid in the community, country or territory where you reside.

(7) Do not connect or disconnect this product while its application products is powered on.

(8) Do not attempt to disassemble or modify this product as it is precision component.

(9) If a part of soldering part has been exposed, and avoid contact (short-circuit) with a metallic part of the case etc. about FPC of this model, please.
Please insulate it with the insulating tape etc. if necessary.
The defective operation is caused, and there is a possibility to generation of heat and the ignition.

(10) Since excess current protection circuit is not built in this TFT module, there is the possibility that LCD module or peripheral circuit become feverish and burned in case abnormal operation is generated.
We recommend you to add excess current protection circuit to power supply.

(11) The devices on the FPC are damageable to electrostatic discharge, because the terminals of the devices are exposed.
Wear grounded wrist-straps and use electrostatic neutralization blowers to prevent static charge and discharge when handling the TFT monitors.
Designate an appropriate operating area, and set equipment, tools, and machines properly when handling this product.

Caution **This mark is used to indicate a precaution or an instruction which, if not correctly observed, may result in bodily injury, or material damages alone.**

16.2 Precautions for Handling

1) Wear finger tips at incoming inspection and for handling the TFT monitors to keep display quality and keep the working area clean.
Do not touch the surface of the monitor as it is easily scratched.

2) Wear grounded wrist-straps and use electrostatic neutralization blowers to prevent static charge and discharge when handling the TFT monitors as the LED in this TFT monitors is damageable to electrostatic discharge.
Designate an appropriate operating area, and set equipment, tools, and machines properly when handling this product.

3) Avoid strong mechanical shock including knocking, hitting or dropping to the TFT monitors for protecting their glass parts. Do not use the TFT monitors that have been experienced dropping or strong mechanical shock.

4) Do not use or storage the TFT monitors at high temperature and high humidity environment.
Particularly, never use or storage the TFT monitors at a location where condensation builds up.

5) Avoid using and storing TFT monitors at a location where they are exposed to direct sunlight or ultraviolet rays to prevent the LCD panels from deterioration by ultraviolet rays.

6) Do not stain or damage the contacts of the FPC cable .
FPC cable needs to be inserted until it can reach to the end of connector slot.
During insertion, make sure to keep the cable in a horizontal position to avoid an oblique insertion.
Otherwise, it may cause poor contact or deteriorate reliability of the FPC cable.

7) The FPC cable is a design very weak to the bend and the pull as it is fixed with the tape.
Do not bend or pull the FPC cable or carry the TFT monitor by holding the FPC cable.

8) Peel off the protective film on the TFT monitors during mounting process.
Refer to the section 14.5 on how to peel off the protective film.
We are not responsible for electrostatic discharge failures or other defects occur when peeling off the protective film.

16.3 Precautions for Operation

1) Since this TFT monitors are not equipped with light shielding for the driver IC, do not expose the driver IC to strong lights during operation as it may cause functional failures.

2) When turning off the power, turn off the input signal before or at the same timing of switching off the power.

3) Do not plug in or out the FPC cable while power supply is switch on.
Plug the FPC cable in and out while power supply is switched off.

4) Do not operate the TFT monitors in the strong magnetic field. It may break the TFT monitors.

5) Do not display a fixed image on the screen for a long time.
Use a screen-saver or other measures to avoid a fixed image displayed on the screen for a long time.
Otherwise, it may cause burn-in image on the screen due the characteristics of liquid crystal.

16.4 Storage Condition for Shipping Cartons

Storage environment

- Temperature: 0 to 40˚C
- Humidity: 60%RH or less
  No-condensing occurs under low temperature with high humidity condition.
- Atmosphere: No poisonous gas that can erode electronic components and/or wiring materials should be detected.
- Time period: 3 months
- Unpacking: To prevent damages caused by static electricity, anti-static precautionary measures (e.g. earthing, anti-static mat) should be implemented.
- Maximum piling up: 7 cartons

16.5 Precautions for Peeling off the Protective film

The followings work environment and work method are recommended to prevent the TFT monitors from static damage or adhesion of dust when peeling off the protective films.

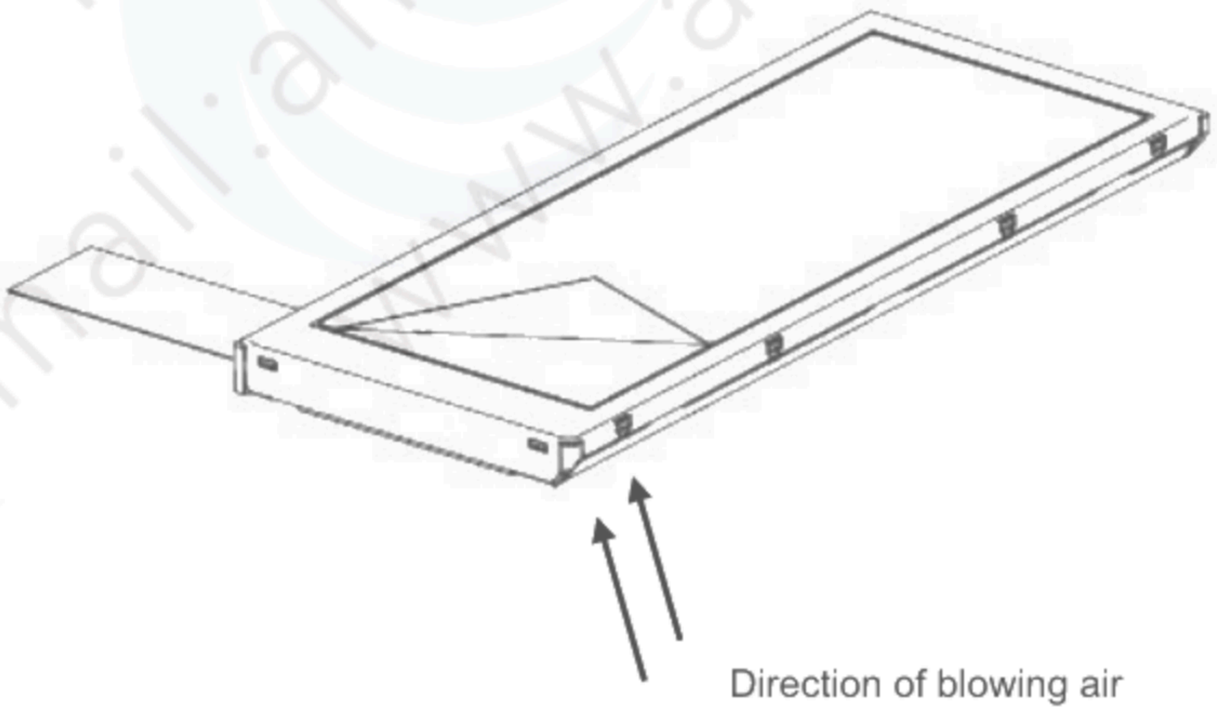
A) Work Environment

a) Humidity: 50 to 70 %RH, Temperature15 to 27˚C
b) Operators should wear conductive shoes, conductive clothes, conductive finger tips and grounded wrist-straps. Anti-static treatment should be implemented to work area's floor.
c) Use a room shielded against outside dust with sticky floor mat laid at the entrance to eliminate dirt.

B) Work Method

The following procedures should taken to prevent the driver ICs from charging and discharging.

a) Use an electrostatic neutralization blower to blow air on the TFT monitors to its lower right when FPC is placed lower left.
   Optimize direction of the blowing air and the distance between the TFT monitors and the electrostatic neutralization blower.
b) Put an adhesive tape (Scotch tape, etc) at the lower right corner area of the protective film to prevent scratch on surface of TFT monitors.
c) Peel off the adhesive tape slowly (spending more than 2 secs to complete) by pulling it to opposite direction.



Direction of blowing air
(Optimize air direction and the distance)

APPENDIX

Reference Method for Measuring Optical Characteristics and Performance

1. Measurement Condition

Measuring instruments: CS1000（KONICA MINOLTA）, LCD7000(OTSUKA ELECTRONICS）,EZcontrast160D（ELDIM）

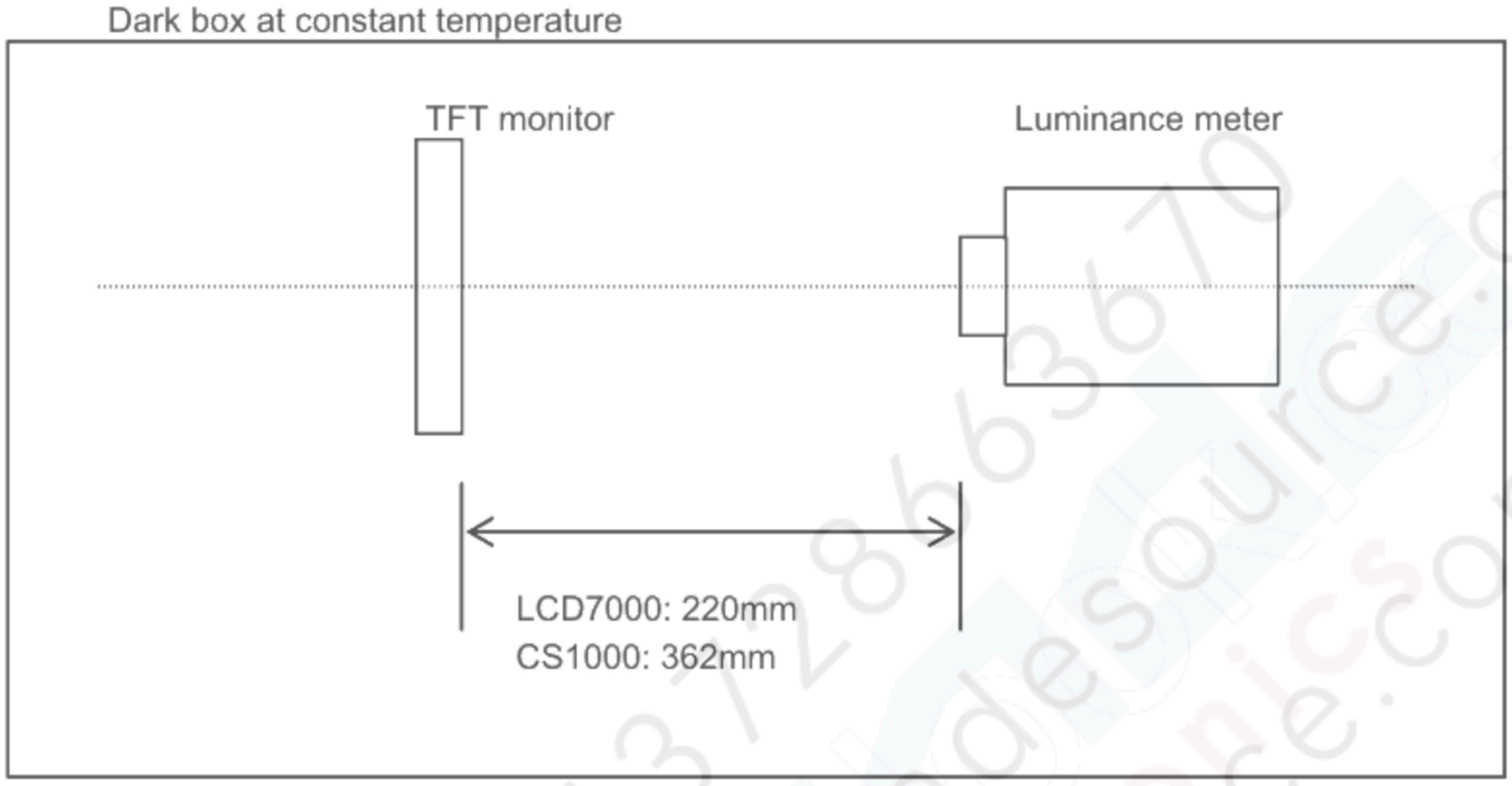
Driving condition: Refer to the section "Optical Characteristics"

Measured temperature: 25°C unless specified

Measurement system: See the chart below. The luminance meter is placed on the normal line of measurement system.

Measurement point: At the center of the screen unless otherwise specified

Dark box at constant temperature

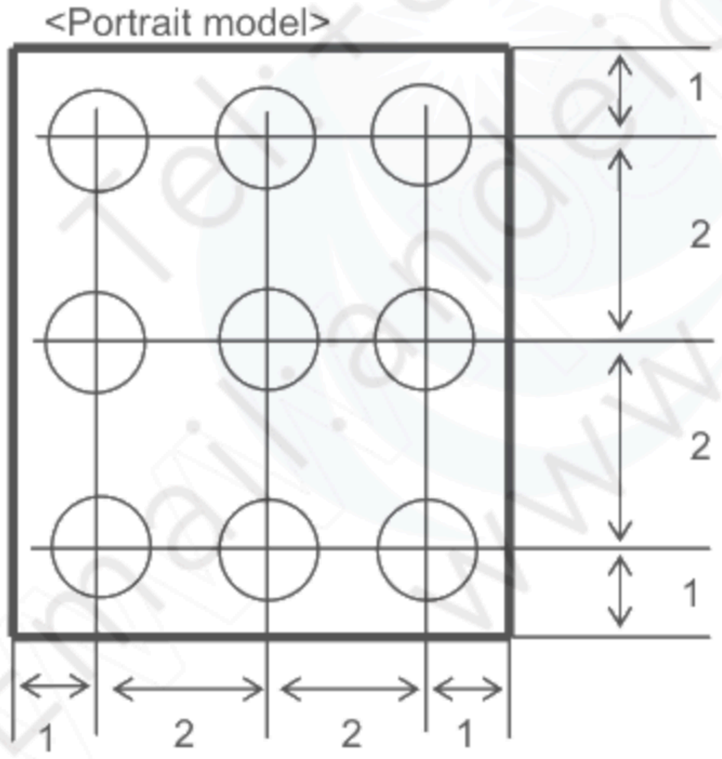


Measurement is made after 30 minutes of lighting of the backlight.

Measurement point: At the center point of the screen

Brightness distribution: 9 points shown in the following drawing.

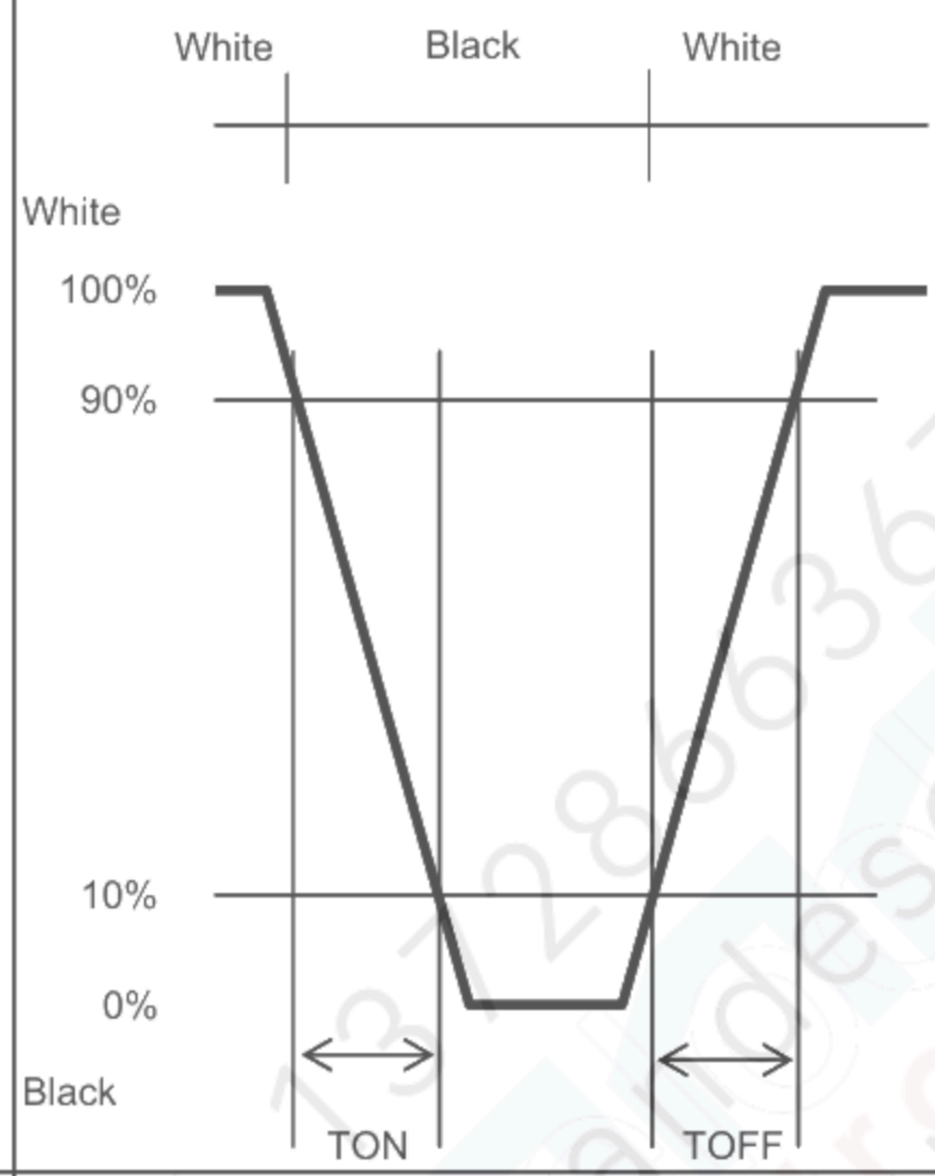
<Portrait model>



Dimensional ratio of active area

Backlight IL=35.0mA

2. Test Method

Notice	Item	Test method	Measuring instrument	Remark
1	Response time	Measure output signal waveform by the luminance meter when raster of window pattern is changed from white to black and from black to white. 	LCD7000	Black display [Data]=00h White display [Data]=3Fh TON Rise time TOFF Fall time
2	Contrast ratio	Measure maximum luminance Y1([Data]=3Fh) and minimum luminance Y2([Data]=00h) at the center of the screen by displaying raster or window pattern. Then calculate the ratio between these two values. Contrast ratio = Y1/Y2 Diameter of measuring point: 8mmφ	CS1000	
3	Viewing angle Horizontalθ Verticalφ	Move the luminance meter from right to left and up and down and determine the angles where contrast ratio is 5.	EZcontrast160D	
4	White chromaticity	Measure chromaticity coordinates x and y of CIE1931 colorimetric system at [Data] = 3Fh Color matching faction: 2°view	CS1000	
5	Burn-in	Visually check burn-in image on the screen after 2 hours of "window display" ([Data]=3Fh/00h).		At optimized VCOMDC
6	Center brightness	Measure the brightness at the center of the screen.	CS1000	
7	Brightness distribution	(Brightness distribution) = 100 x B/A % A : max. brightness of the 9 points B : min. brightness of the 9 points	CS1000	