INNOLUX DISPLAY CORPORATION

FOG

SPECIFICATION

Customer: _____

Model Name: HE080IA-06B

Date: 2013/11/29

Version: V01

■Preliminary Specification
□Final Specification

For Customer's Acceptance

Approved by	Comment

Approved by	Reviewed by	Prepared by
Henry Hsiung	Wang Wenyi	Wang Yifan

Record of Revision

Version	Revise Date	Page	Content
V01	2013/11/29	ALL	Initial Release.

Contents

1. General Specifications

No.	Item	Specification	Remark
1	LCD size	8.0 inch diagonal	
2	Driver element	a-Si TFT active matrix	
3	Resolution	800 × 3(RGB) × 1280	
4	Display mode	Normally Black, Transmissive	
5	Dot pitch	0.04485(W) × 0.13455(H)mm	
6	Active area	107.640(W) × 172.224(H)mm	
7	Panel size	112.64 × 181.80 × 1.07 (D) mm	Note 1
8	Surface treatment	Hard Coating	
9	Color arrangement	RGB-stripe	
10	View direction(Gray Inversion)	Free	
11	Interface	MIPI	
12	Panel power consumption	0.45W	
13	Weight	TBD	

Note 1: Refer to Mechanical Drawing.

2. Pin Assignment

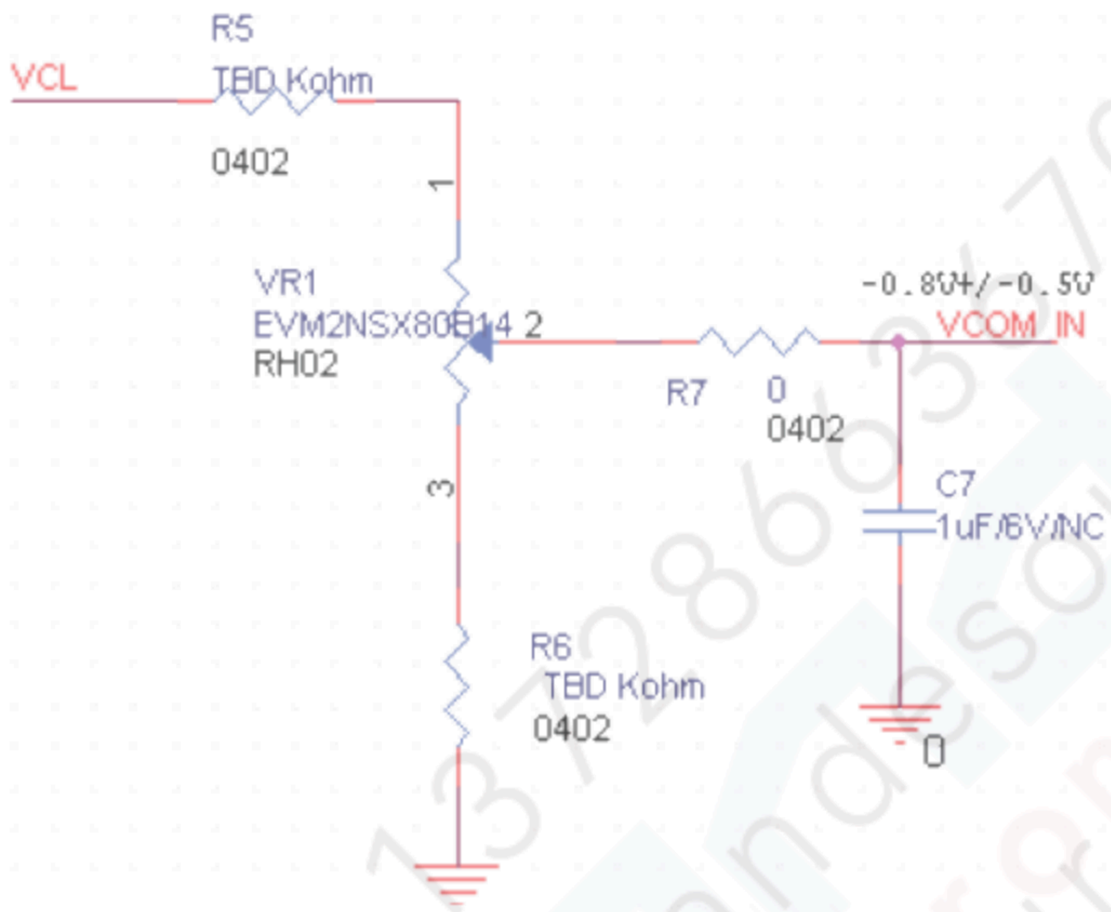
A 40pin connector is used for the module electronics interface.In this model used "FH33J-40S-0.5SH(10)" manufactured by Hirose or the same package connector.

Pin No.	Symbol	Description	Remark
1	VCOM	Common Voltage(-0.8 ± 0.5V)	Note 1
2	VDDIN	Power supply for interface system except MIPI interface pin,VDDIN=1.8V	
3	VDDIN		
4	GND	GROUND	
5	RST	Device reset signal	Note 2
6	NC	No connection	
7	GND	GROUND	
8	MIPI_0N	MIPI Negative data signal (-)	
9	MIPI_0P	MIPI Positive data signal (+)	
10	GND	GROUND	
11	MIPI_1N	MIPI Negative data signal (-)	
12	MIPI_1P	MIPI Positive data signal (+)	
13	GND	GROUND	
14	MIPI_CKN	MIPI Negative clock signal (-)	
15	MIPI_CKP	MIPI Positive clock signal (+)	
16	GND	GROUND	
17	MIPI_2N	MIPI Negative data signal (-)	
18	MIPI_2P	MIPI Positive data signal (+)	
19	GND	GROUND	
20	MIPI_3N	MIPI Negative data signal (-)	
21	MIPI_3P	MIPI Positive data signal (+)	
22	GND	GROUND	
23	NC	No connection	
24	NC	No connection	
25	GND	GROUND	
26	NC	No connection	
27	PWMO	PWM control signal for LED driver (CABC)	
28	NC	No connection	
29	VCL	Output voltage pin,use it to generate Vcom voltage by a VR circuit (output voltage -2.5V)	
30	GND	GROUND	
31	LED-	LED cathode	
32	LED-		
33	NC	No connection	
34	NC	No connection	
35	AVEE	Analog supply negative voltage	

36	NC	No connection	
37	NC	No connection	
38	AVDD	Analog supply positive voltage	
39	LED+	LED anode	
40	LED+		

I: input, O: output, P: Power

Note1:Typical VCOM is only a reference value,it must be optimized according to each LCM,Be sure to use VR



Note 2: Global reset pin.Active Low to enter Reset State.Normally pull high.suggest to connecting withan RC reset circuit for stability.

3. Operation Specifications

3.1. Absolute Maximum Ratings

(Note 1)

Item	Symbol	Values		Unit	Remark
		Min.	Max.		
Power voltage	VDDIN	-0.3	5.5	V	
	AVDD	-0.3	6.6	V	
	AVEE	+0.3	-6.6	V	

Note 1: The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

3.2.Typical Operation Conditions

(GND=0V)

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power voltage	VDDIN	1.7	1.8	1.9	Power voltag	VDDIN
	AVDD	5.4	(6.0)	6.0		AVDD
	AVEE	-6.0	(-6.0)	-5.4		AVEE
Input logic high voltage	V_{IH}	0.7VDDIN	-	VDDIN	Input logic	V_{IH}
Input logic low voltage	V_{IL}	0	-	0.3VDDIN	Input logic	V_{IL}

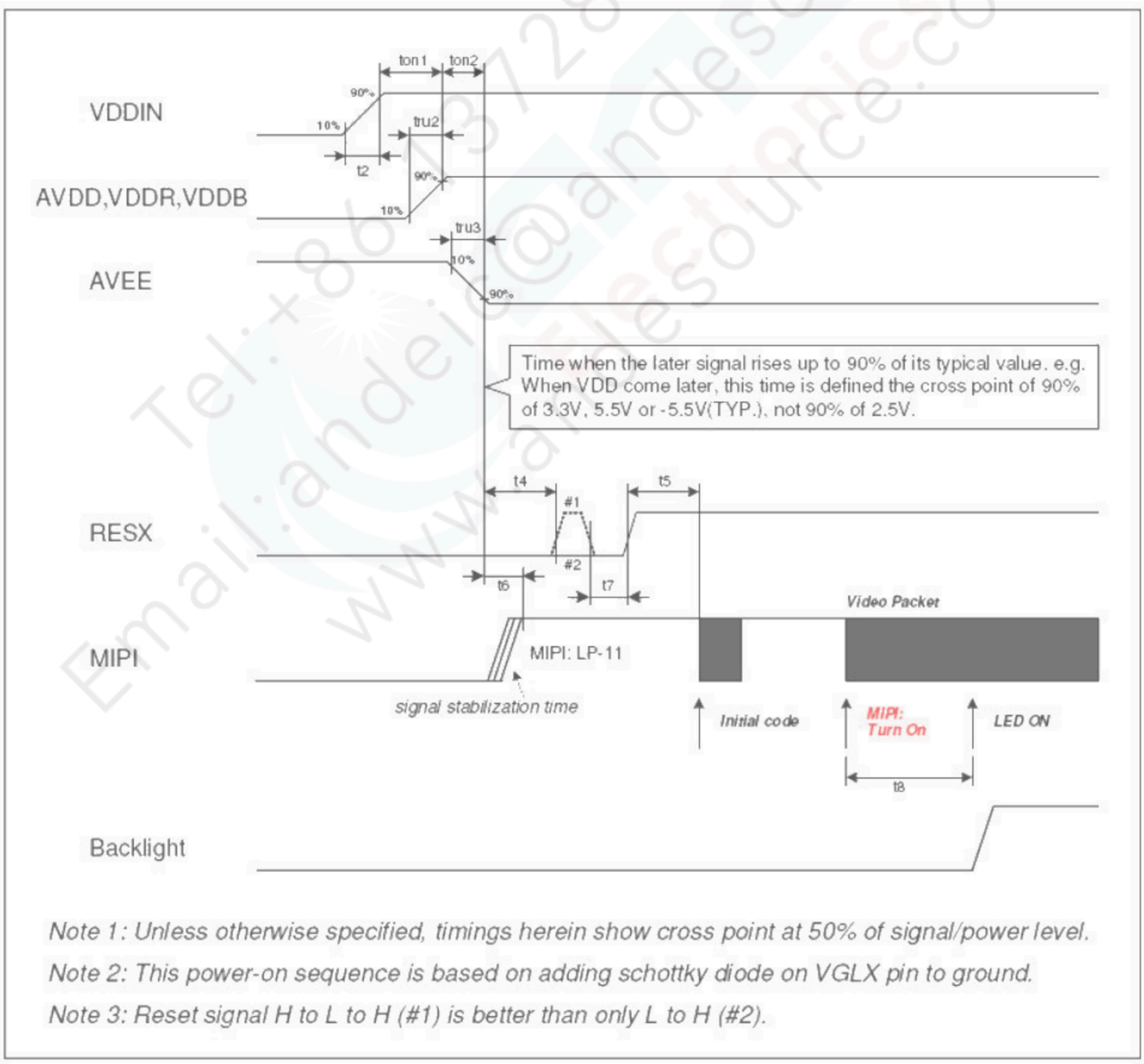
3.3. Current Consumption

(GND=AV_{SS}=0V)

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Current for Driver	I_{VDDIN}	-	(TBD)	-	mA	
	I_{AVDD}	-	(TBD)	-	mA	
	I_{AVEE}	-	(TBD)	-	mA	

3.4. Power Sequence

a. Power on:



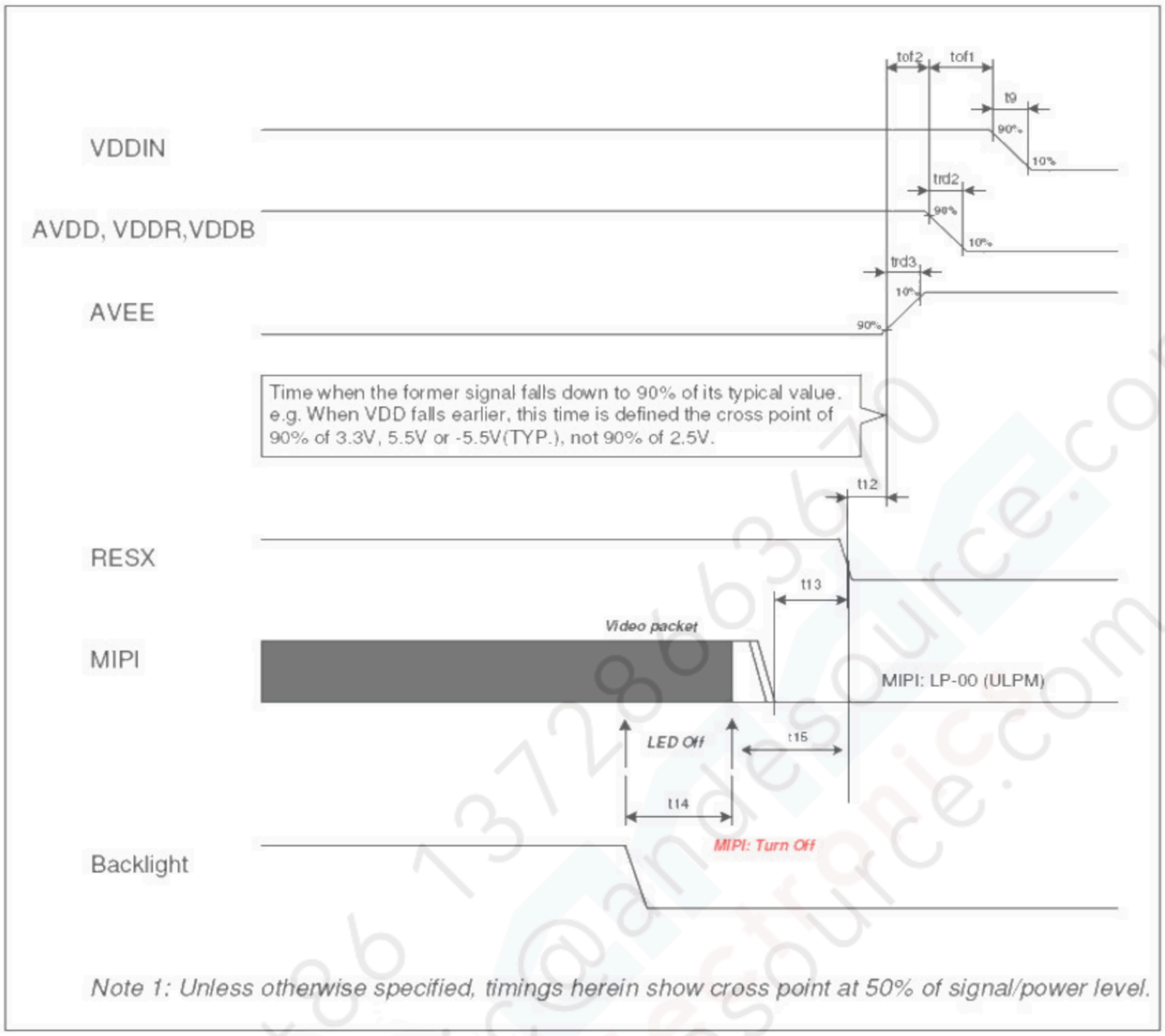
Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Note 2: This power-on sequence is based on adding schottky diode on VGLX pin to ground.

Note 3: Reset signal H to L to H (#1) is better than only L to H (#2).

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
ton1		No limit		ms	
ton2		0(Note)		ms	
ton3		No limit	-	ms	
ton4		No limit	-	ms	
t2			150	μs	
tru1			150	μs	
tru2			150	μs	
tru3			150	μs	
tru4			150	μs	
t4	40	-	-	ms	
t5	120			ms	
t6	0			ms	
t7	10			μs	
t8	8			VS	Keep data more than 8 frames (VS)

b. Power off:



Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
t9	150			μs	
tof1		No limit		ms	
tof2		0(Note)	-	ms	
tof3		No limit	-	ms	
tof4		No limit		ms	
trd1	150			μs	
trd2	150			μs	
trd3	150			μs	
trd4	150			μs	
t12	0		-	ms	
t13	0			ms	
T14	0			ms	
T15	10			ms	

3.5. MIPI interface (Mobile Industry Processing Interface)

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode.

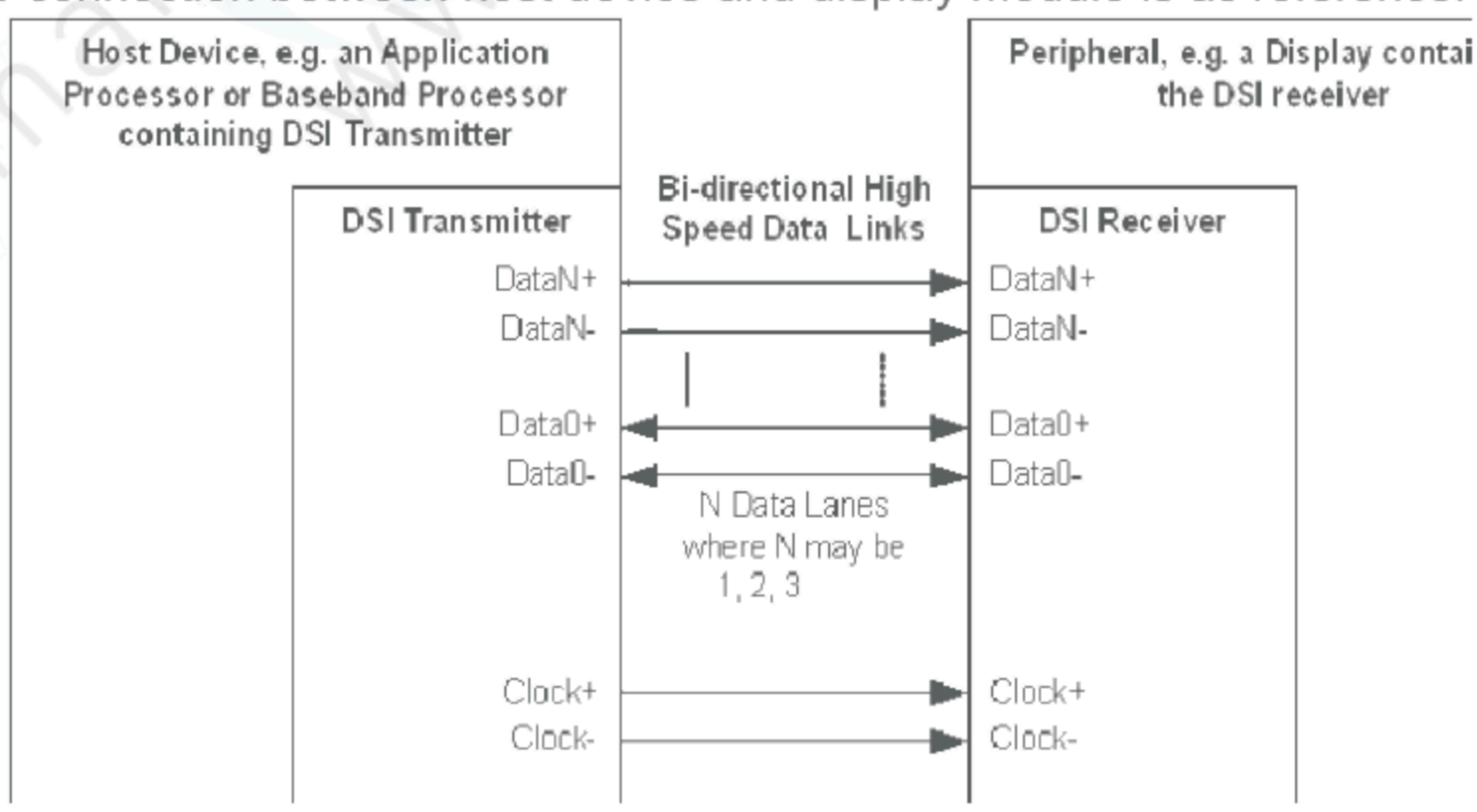
Note: The product only supports Video Mode operation.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

3.5.1. MIPI Lane Configuration

	MCU (Master) Display Module (Slave)
Clock Lane+/-	Unidirectional Lane ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane0+/-	Bi-directional Lane ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT
Data Lane1+/-	Unidirectional ■ Forward High speed
Data Lane2+/-	Unidirectional ■ Forward High speed
Data Lane3+/-	Unidirectional ■ Forward High speed

The connection between host device and display module is as reference.



3.6. MIPI Signal Timing Characteristics

3.6.1. AC Electrical Characteristics

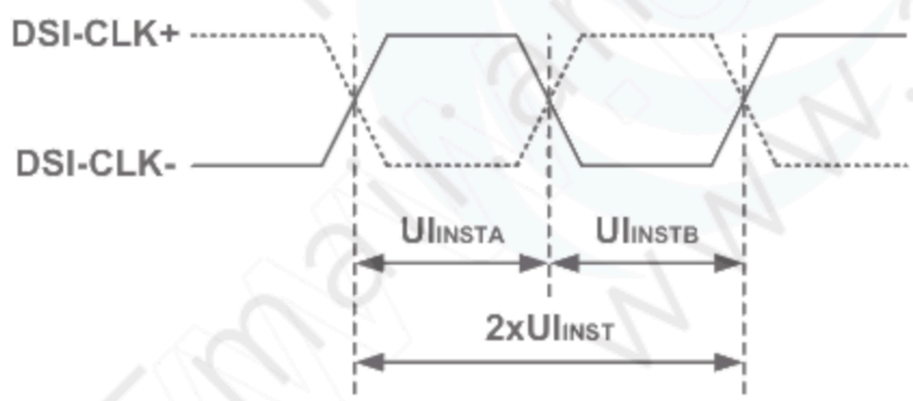
3.6.1.1 High Speed Mode

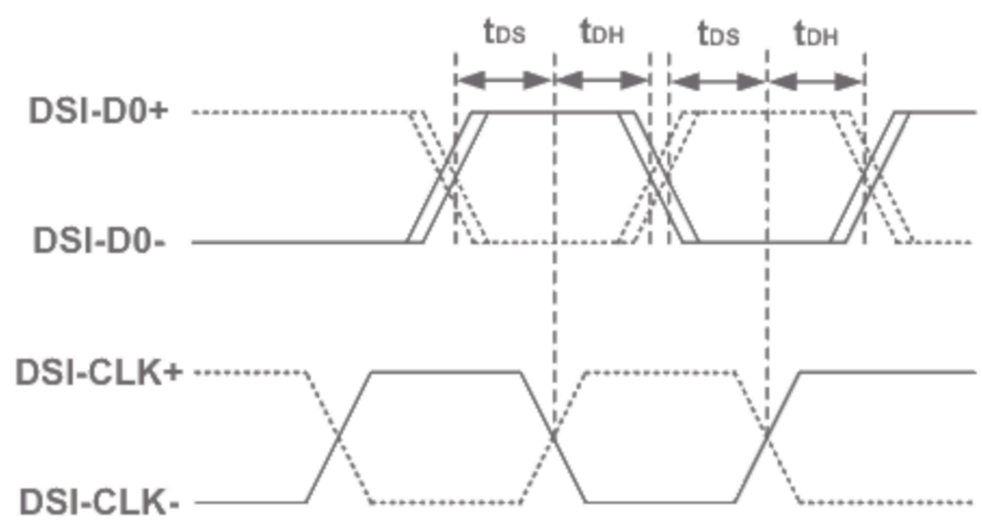
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	2xUIINST	Double UI instantaneous	4	-	8	ns	4 Lane (Note 2)
			3	-	8	ns	3 Lane (Note 2)
			2.352	-	8	ns	2 Lane (Note 3)
DSI-CLK+/-	UIINSTA UIINSTB	UI instantaneous halfs (UI = UIINSTA = UIINSTB)	2	-	4	ns	4 Lane (Note 2)
			1.5	-	4	ns	3 Lane (Note 2)
			1.176	-	4	ns	2 Lane (Note 3)
DSI-Dn+/-	tDS	Data to clock setup time	0.15x UI	-	-	ps	
DSI-Dn+/-	tDH	Data to clock hold time	0.15x UI	-	-	ps	
DSI-CLK+/-	tDRTCLK	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	tDRTDATA	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	tDFTCLK	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	tDFTDATA	Differential fall time for data	150	-	0.3xUI	ps	

Note 1) Dn = D0, D1, D2 and D3.

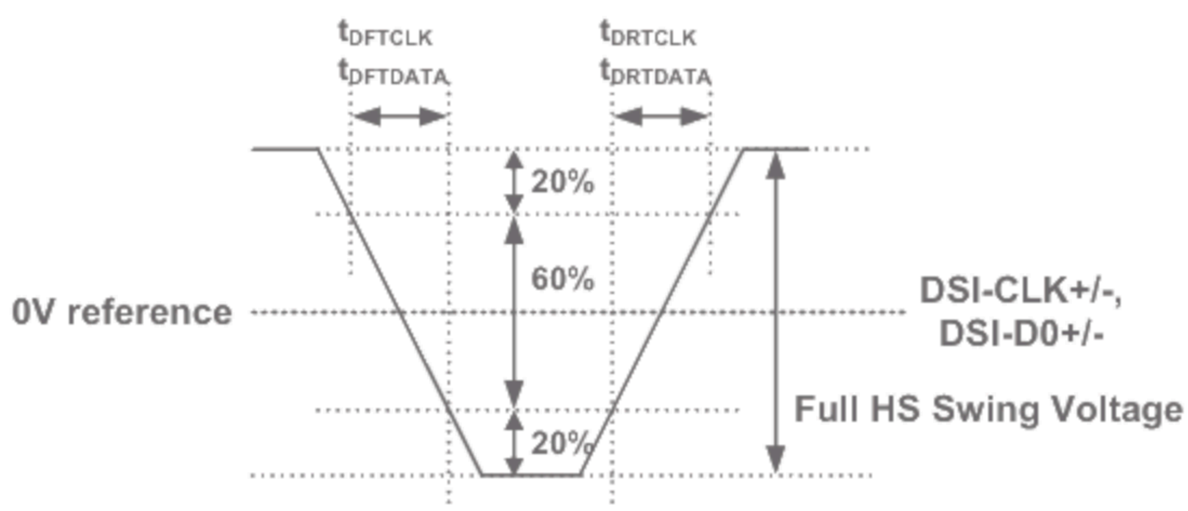
Note 2) Maximum total bit rate is 2Gbps for 24-bit data format, 1.5Gbps for 18-bit data format and 1.33Gbps for 16-bit data format in 3 lanes or 4 lanes application which support to 800RGBx 1280 resolution.

Note 3) Maximum total bit rate is 1.7Gbps for 24-bit data format, 1.275Gbps for 18-bit data format and 1.13Gbps for 16-bit data format in 2 lanes application which support to 720RGBx1280 resolution.





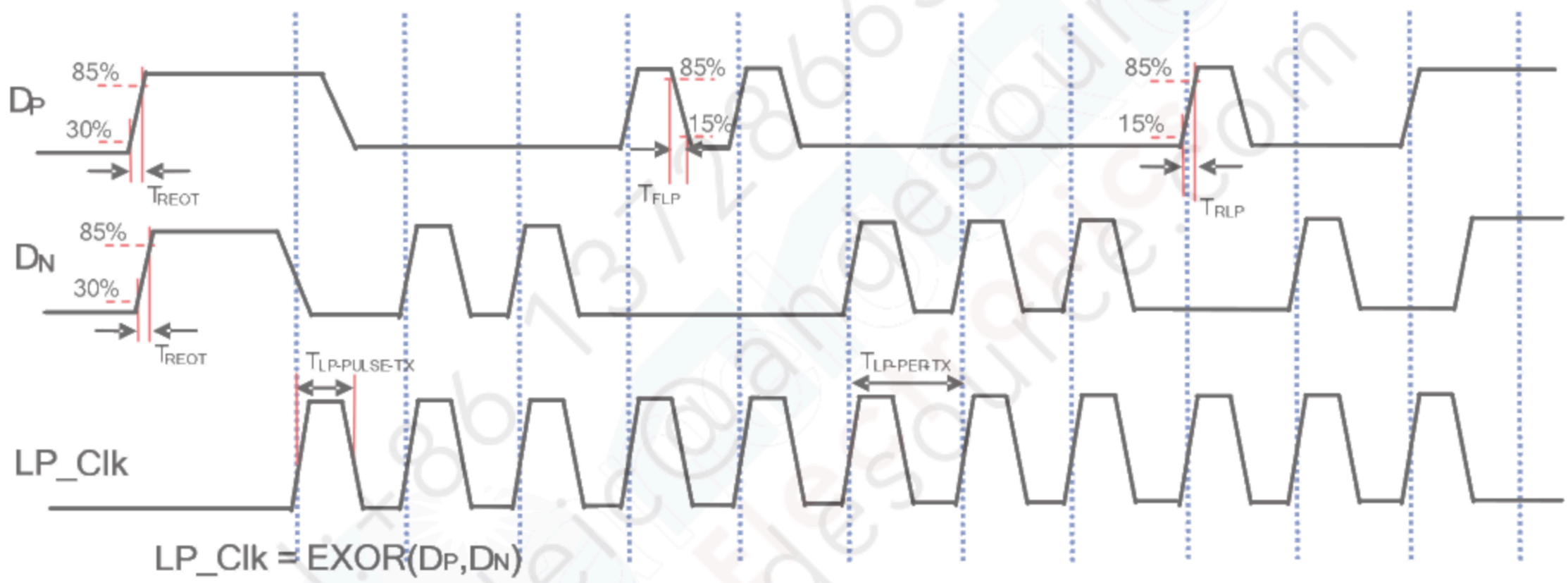
DSI clock channel timing



Rising and fall time on clock and data channel

3.6.1.2 LP Transmission

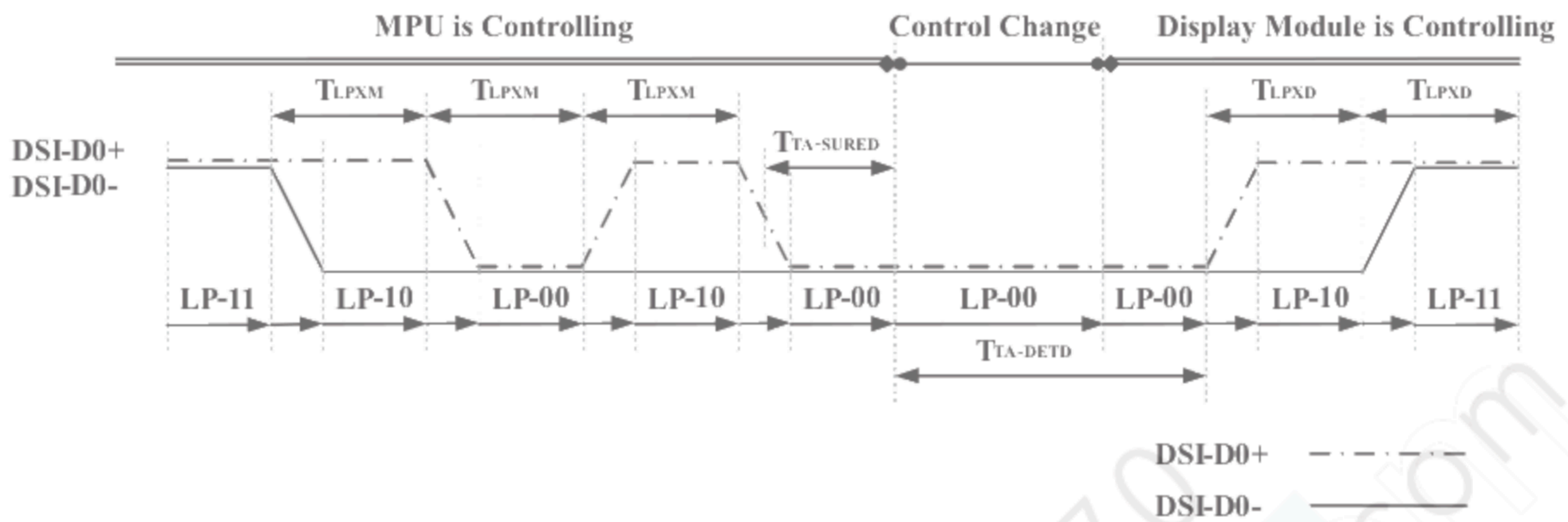
Parameter	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
DSI CLK frequency(LP)	F_{DSICLK_LP}			10	MHz	
DSI CLK Cycle Time(LP)	t_{CLKC_LP}	100			ns	
DSI Data Transfer Rate(LP)	t_{DSIR_LP}			10	Mbps	
15%-85% rise time and fall time	T_{RLP} / T_{FLP}	-	-	35	ns	
30%-85% rise time(from HS to LP)	T_{REOT}	-	-	35	ns	
Pulse width of the LP exclusive-OR clock	$t_{LP\text{-}PULSE\text{-}TX}$	50	65	-	ns	
Period of the LP exclusive-OR clock	$t_{LP\text{-}PRE\text{-}TX}$	100	130	-	ns	

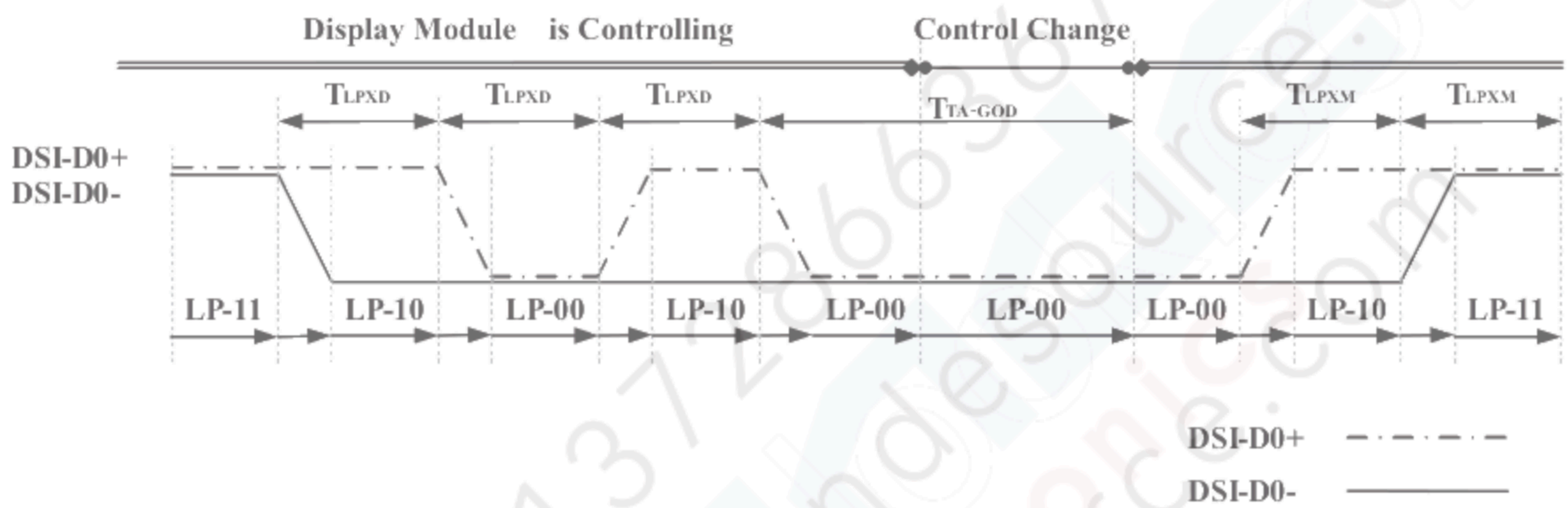


3.6.1.3 Low Power Mode

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+ /-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU (Display Module	50	-	75	ns	Input
DSI-D0+ /-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (MPU	50	-	75	ns	Output
DSI-D0+ /-	TTA-SURED	Time-out before the MPU start driving	TLPXD	-	2xTLPXD	ns	Output
DSI-D0+ /-	TTA-GETD	Time to drive LP-00 by display module	5xTLPXD	-	-	ns	Input
DSI-D0+ /-	TTA-GOD	Time to drive LP-00 after turnaround request - MPU	4xTLPXD	-	-	ns	Output

Bus Turnaround (BAT) from MPU to display module Timing





Bus Turnaround (BAT) from display module to MPU Timing

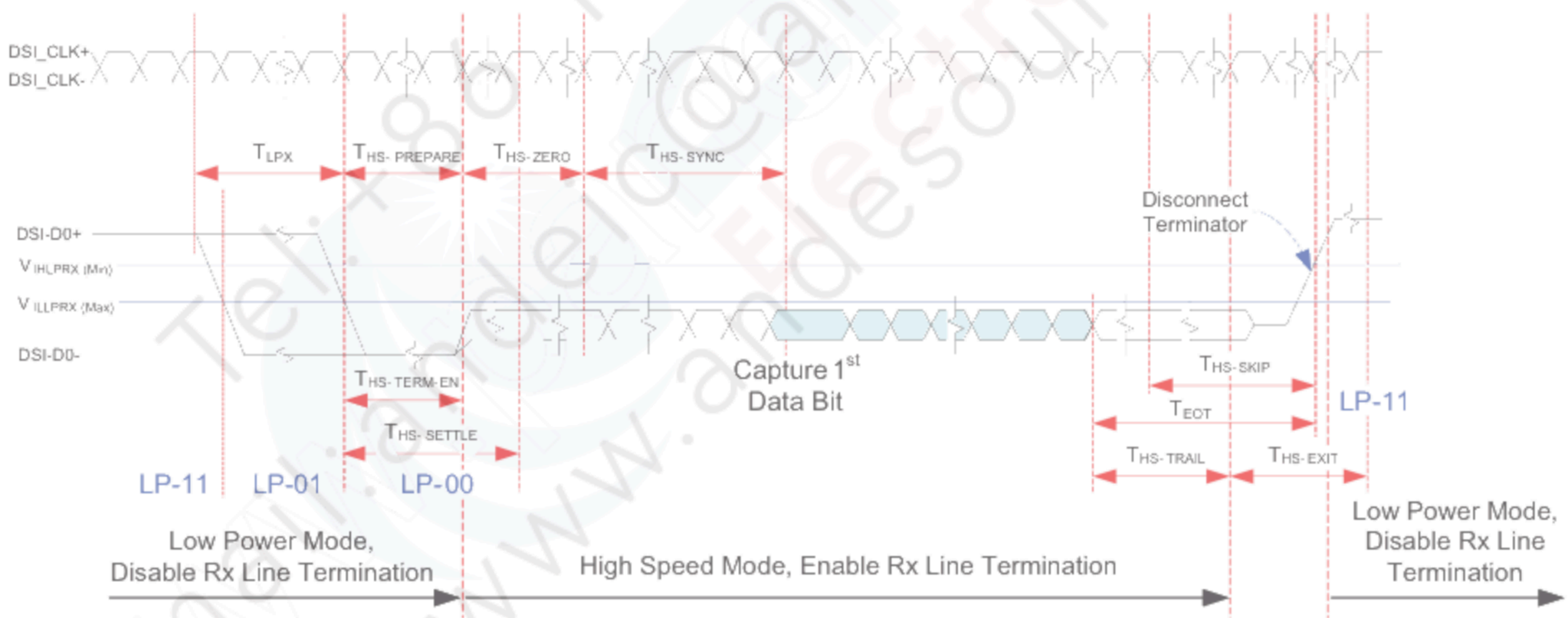
3.6.1.4 DSI Bursts

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to	60+52xUI	-	-	ns	Input

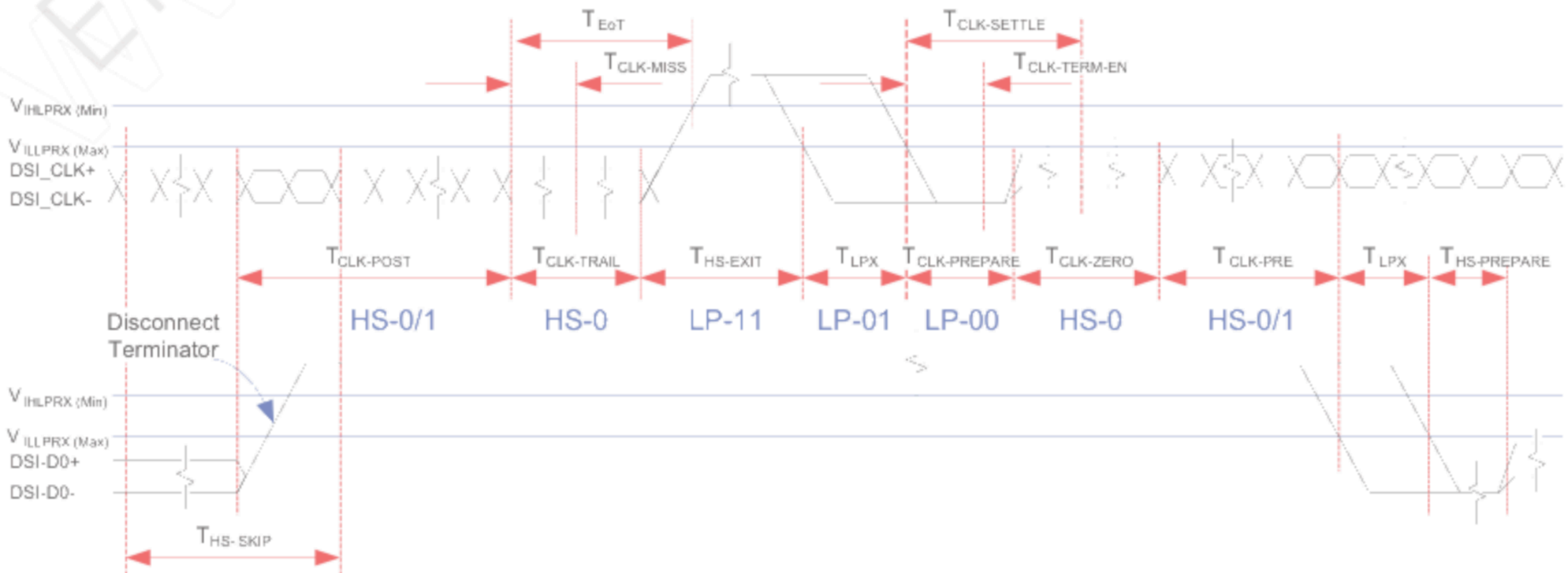
		LP mode					
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE+ TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Two HS transmission can be sent with a break as short as THS-EXIT from each other in continuous clock mode. In discontinuous mode, the break is longer which account TCLK-POS, TCLK-TRAIL and THS-EXIT, before activity in clock and data lanes again.

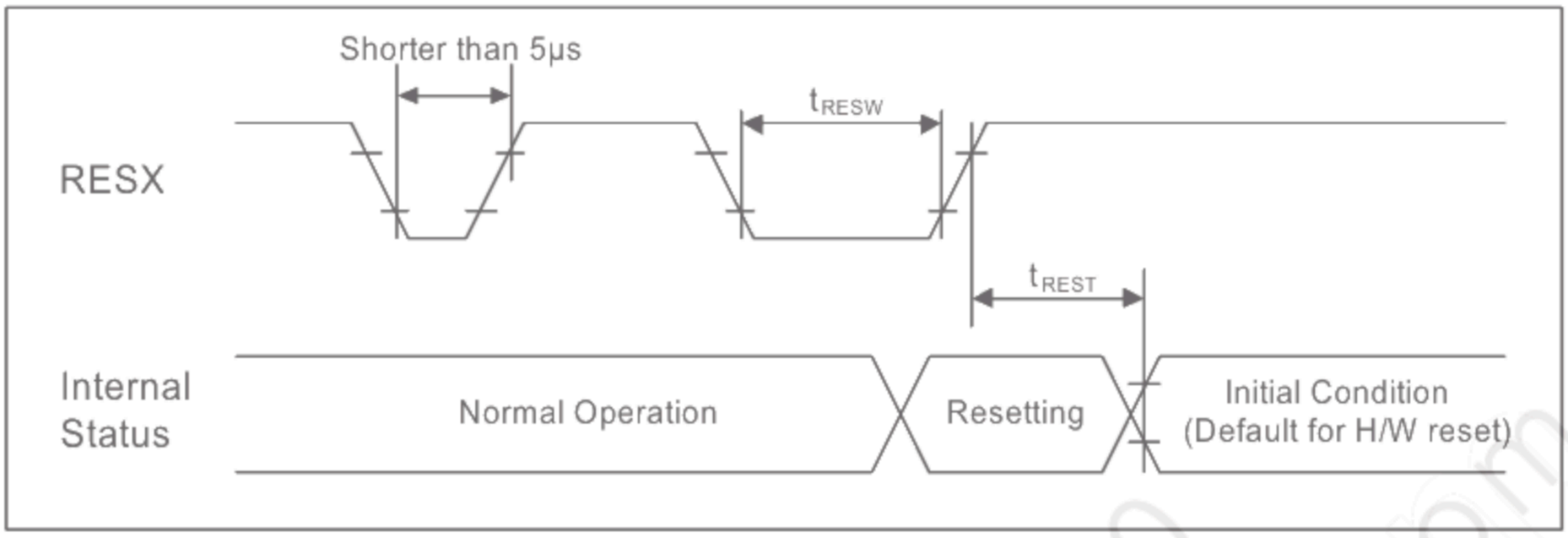


Data lanes-Low Power Mode to/from High Speed Mode Timing



Clock lanes- High Speed Mode to/from Low Power Mode Timing

3.6.1.5 Reset Input Timing



Reset input timing
(VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	t_{RESW}	Reset "L" pulse width (Note 1)	10	-	-	μs	
	t_{REST}	Reset complete time (Note 2)	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode and Note 5

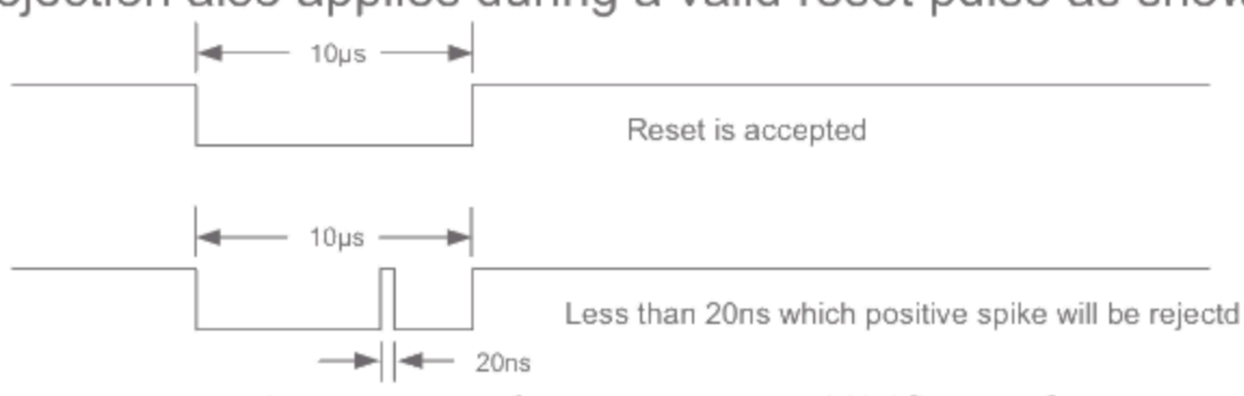
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset Start

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

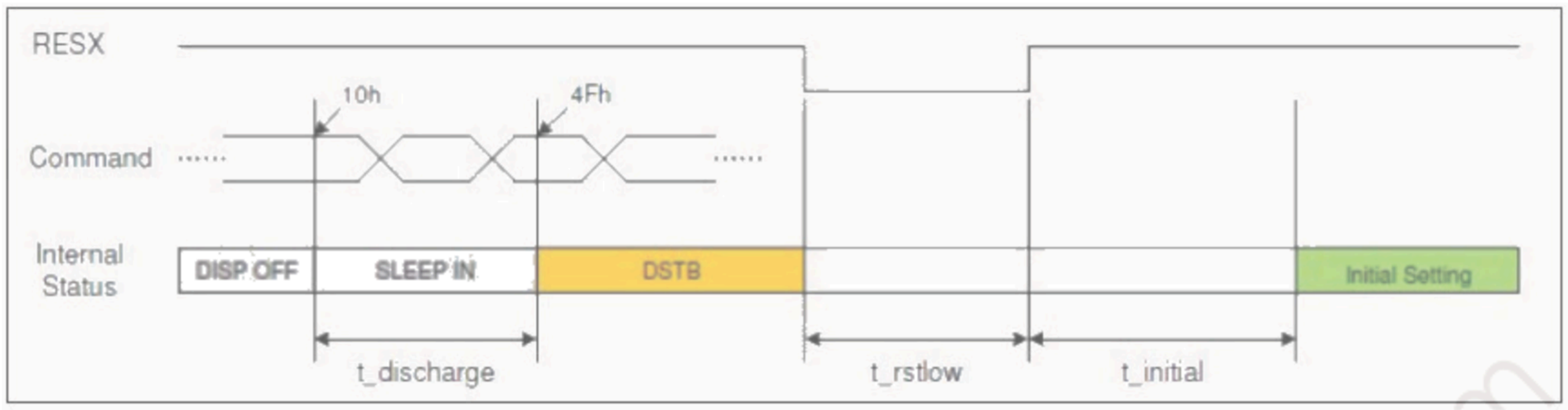
Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4) Spike Rejection also applies during a valid reset pulse as shown below:



Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

3.6.1.6 Deep Standby Mode Timing



(***VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V***,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	tdischarge	Sleep in into DSTB delay time	-	-	100	ms	
	trstlow	Reset low pulse	3	-	-	ms	
	tinitial	Reset high to initial setting delay time	-	-	120	ms	

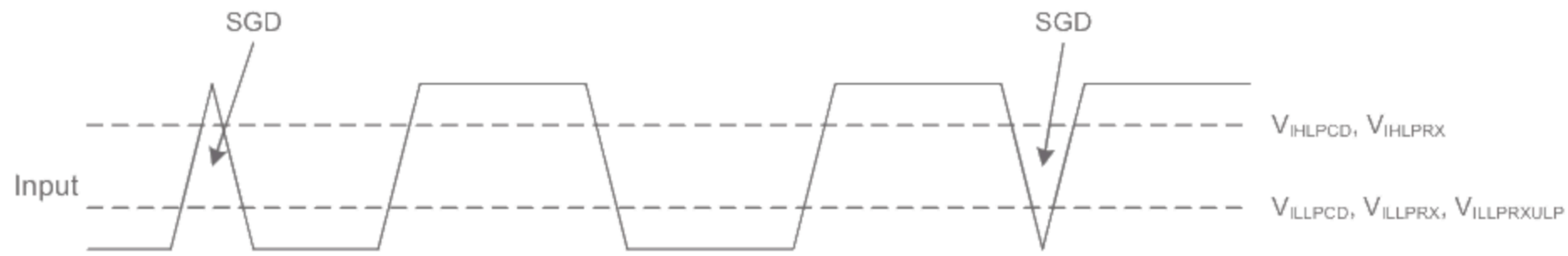
Note 1) t_discharge suggested delay time over 100ms.
Note 2) t_initial suggested delay time over 120ms..

3.6.2. DC Electrical Characteristics

3.6.2.1 DC Characteristics for DSI LP Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK, D0, D1)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0, D1)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic high level input current	I_{IH}	LP-CD, LP-RX	-	-	10	μA
Logic low level input current	I_{IL}	LP-CD, LP-RX	-10	-	-	μA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	300	Vps

Note 1) VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V, Ta=-30 to 70 ºC (to +85 ºC no damage)
Note 2) DSI high speed is off.
Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.

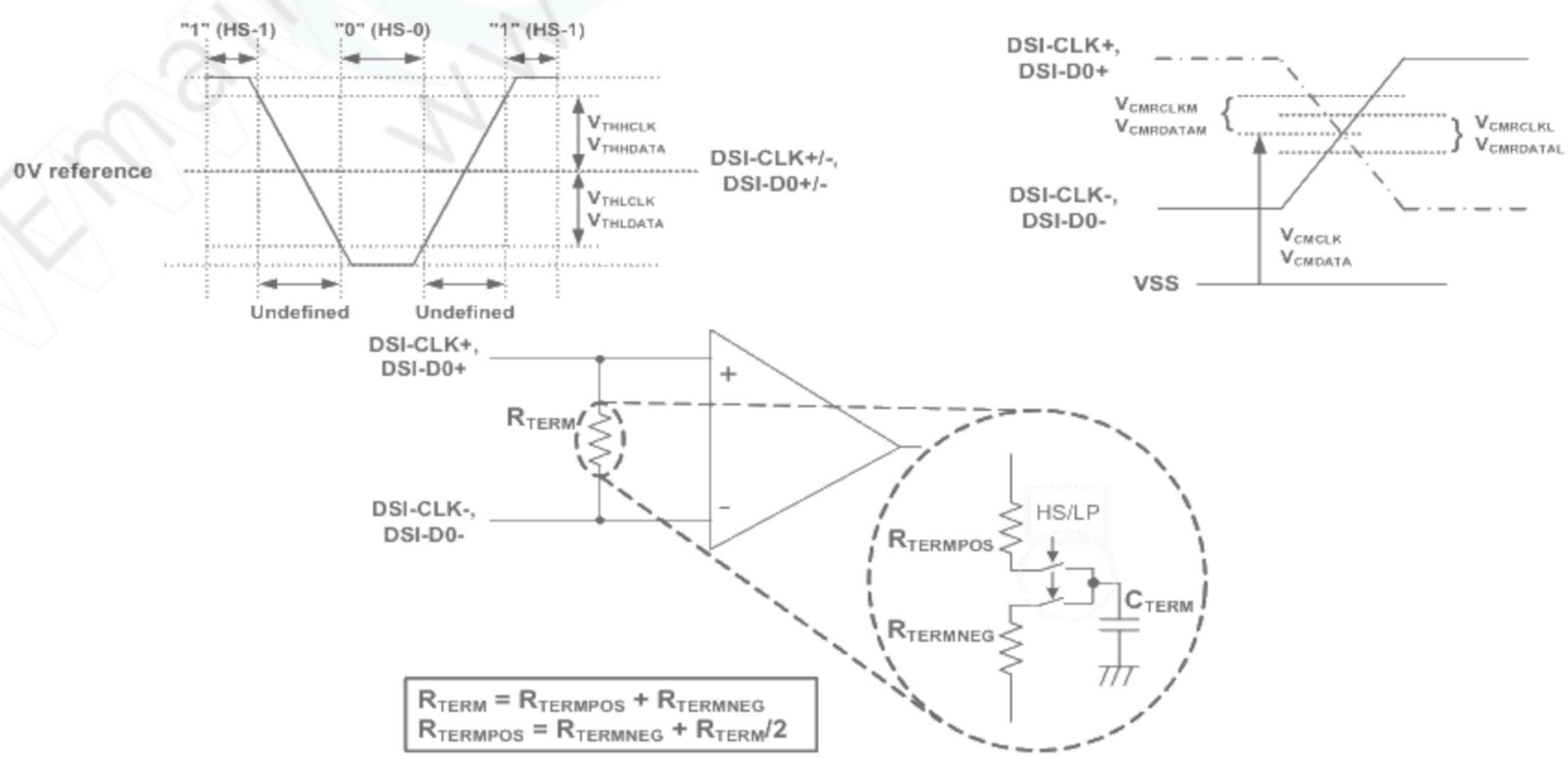


Spike/Glitch rejection-DSI

3.6.2.2 DC Characteristics for DSI HS Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Input voltage common mode range	VCMCLK VCMDATA	DSI-CLK+/-, DSI-Dn+/- (Note2, 3)	70	-	330	mV
Input voltage common mode variation (≤ 450MHz)	VCMRCLKL VCMRDATAL	DSI-CLK+/-, DSI-Dn+/- (Note 4)	-50	-	50	mV
Input voltage common mode variation (≥ 450MHz)	VCMRCLKM VCMRDATAM	DSI-CLK+/-, DSI-Dn+/-	-	-	100	mV
Low-level differential input voltage threshold	VTHLCLK VTHLDATA	DSI-CLK+/-, DSI-Dn+/-	-70	-	-	mV
High-level differential input voltage threshold	VTHHCLK VTHHDATA	DSI-CLK+/-, DSI-Dn+/-	-	-	70	mV
Single-ended input low voltage	VILHS	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-40	-	-	mV
Single-ended input high voltage	VIHHS	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	460	mV
Differential input termination resistor	RTERM	DSI-CLK+/-, DSI-Dn+/-	80	100	125	Ω
Single-ended threshold voltage for termination enable	VTERM-EN	DSI-CLK+/-, DSI-Dn+/-	-	-	450	mV
Termination capacitor	CTERM	DSI-CLK+/-, DSI-Dn+/-	-	-	14	pF

Note 1) VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V, Ta=-30 to 70 ºC (to +85 ºC no damage).
Note 2) Includes 50mV (-50mV to 50mV) ground difference.
Note 3) Without VCMRCLKM / VCMRDATAM.
Note 4) Without 50mV (-50mV to 50mV) ground difference.
Note 5) Dn=D0, D1, D2 and D3.



Differential voltage range, termination resistor and Common mode voltage

4. Optical Specifications.

Note: The optical specifications are measured base on INNOLUX LCM

Item	Symbol	Condition	Values			Unit	Remark
			Min.	Typ.	Max.		
Viewing angle (CR≥ 10)	θ_L	Φ=180°(9 o'clock)		85	-	degree	Note 1f
	θ_R	Φ=0°(3 o'clock)		85	-		
	θ_T	Φ=90°(12 o'clock)		85	-		
	θ_B	Φ=270°(6 o'clock)		85	-		
Response time	$T_{R+} T_F$	Normal θ=Φ=0°	-	25	30	msec	Note 3
Contrast ratio	CR		600	800	-	-	Note 4
Color chromaticity	W_X		0.28	0.31	0.34		Note 2 Note 5 Note 6
	W_Y		0.28	0.33	0.36		
NTSC			55	60		%	
Transmittance	T		4.3		5	%	

Test Conditions:
The test systems refer to Note 2.

Note 1: Definition of viewing angle range

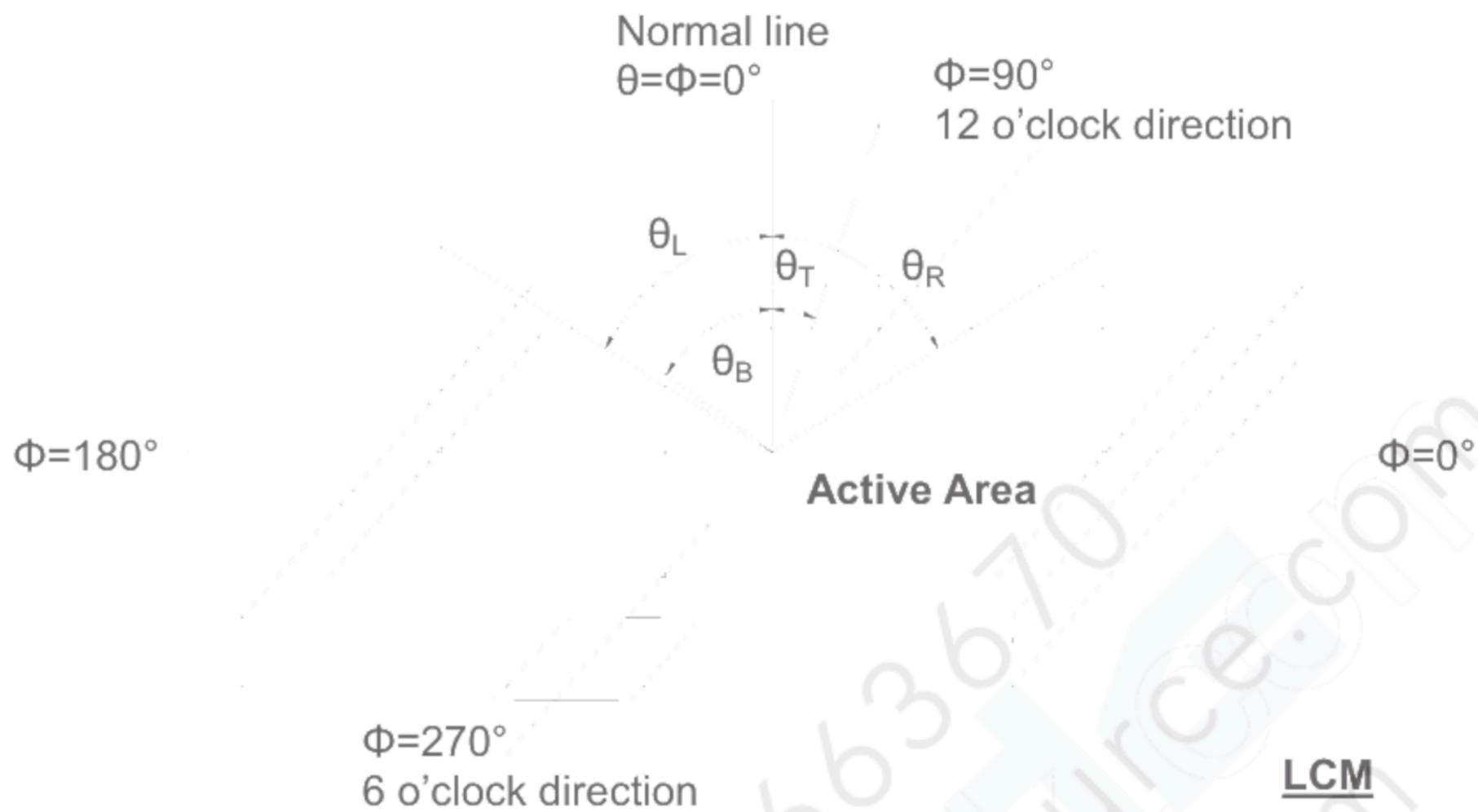
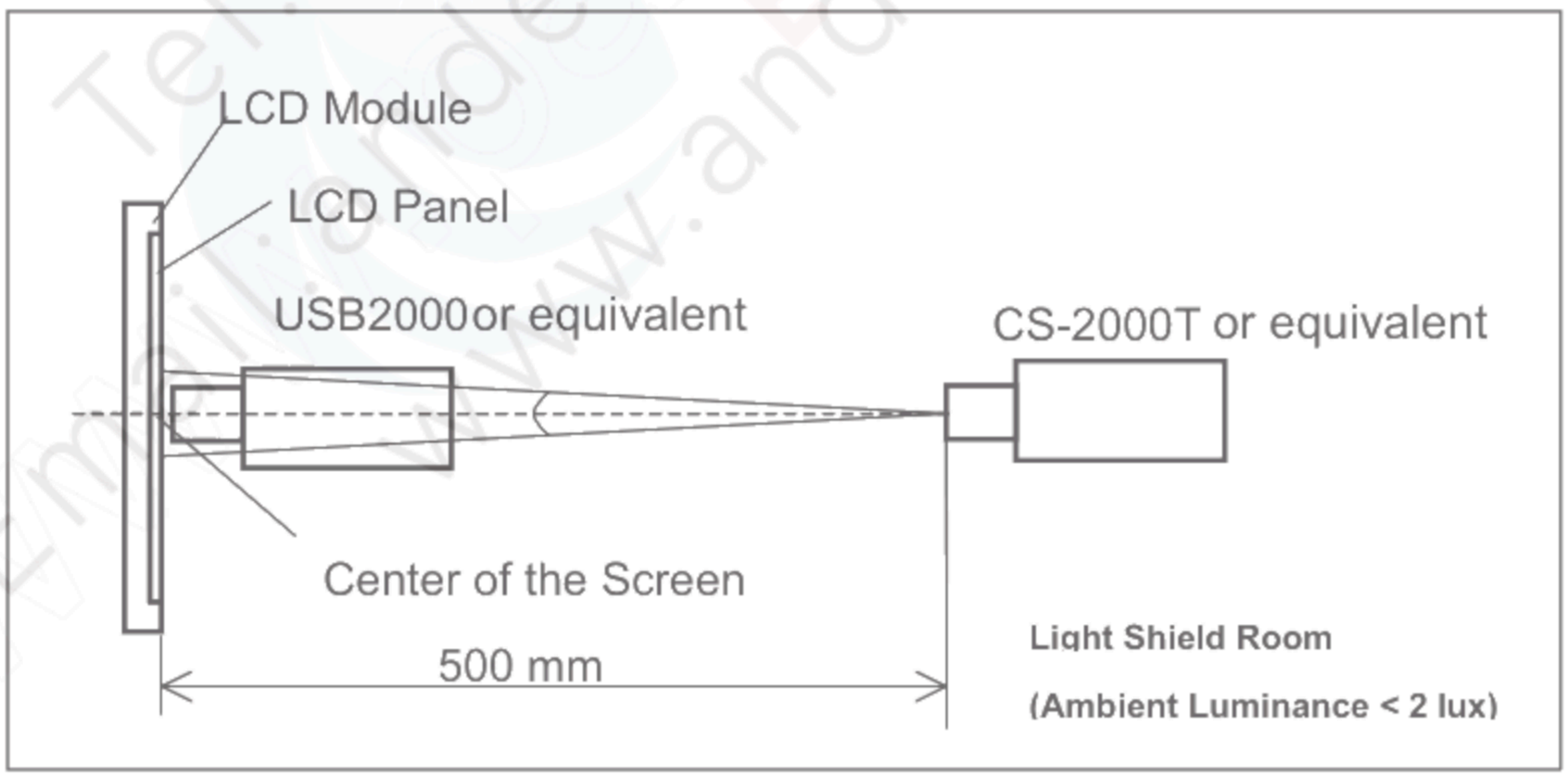


Fig. 4-1 Definition of viewing angle

Note 2: Definition of optical measurement system.
The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Viewing angle is measured by ELDIM-EZ contrast/Height :1.2mm, Response time is measured by Photo detector TOPCON BM-7, other items are measured by BM-5A/ Field of view: 1° /Height: 500mm.)



Note 3: Definition of Response time
The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.

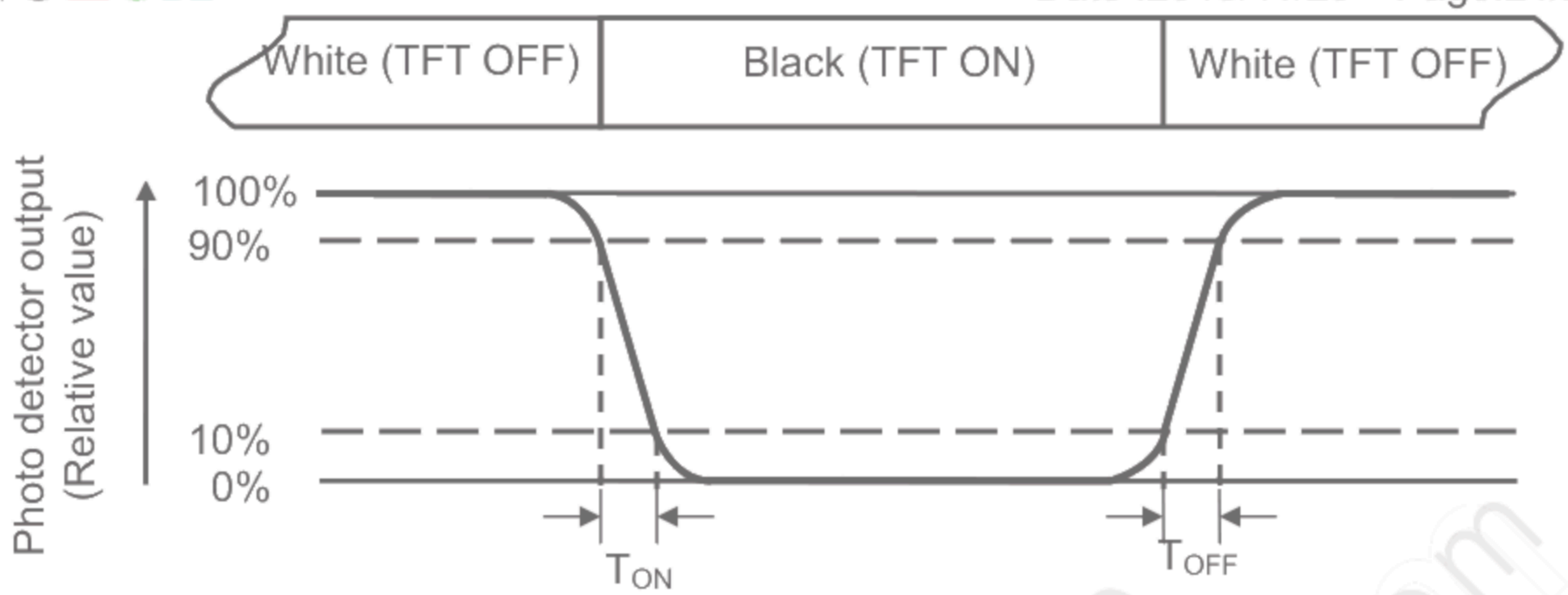


Fig. 4-3 Definition of response time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of color chromaticity (CIE1931)
Color coordinates measured at center point of LCD.

Note 6: All input terminals LCD panel must be ground while measuring the center area of the panel.

Note 7: Definition of Luminance Uniformity
Active area is divided into 9 measuring areas (Refer to Fig. 4-4).Every measuring point is placed at the center of each measuring area.

$$Luminance\ \ Uniformity\ (Yu) = \frac{B_{min}}{B_{max}}$$

L-------Active area length W----- Active area width

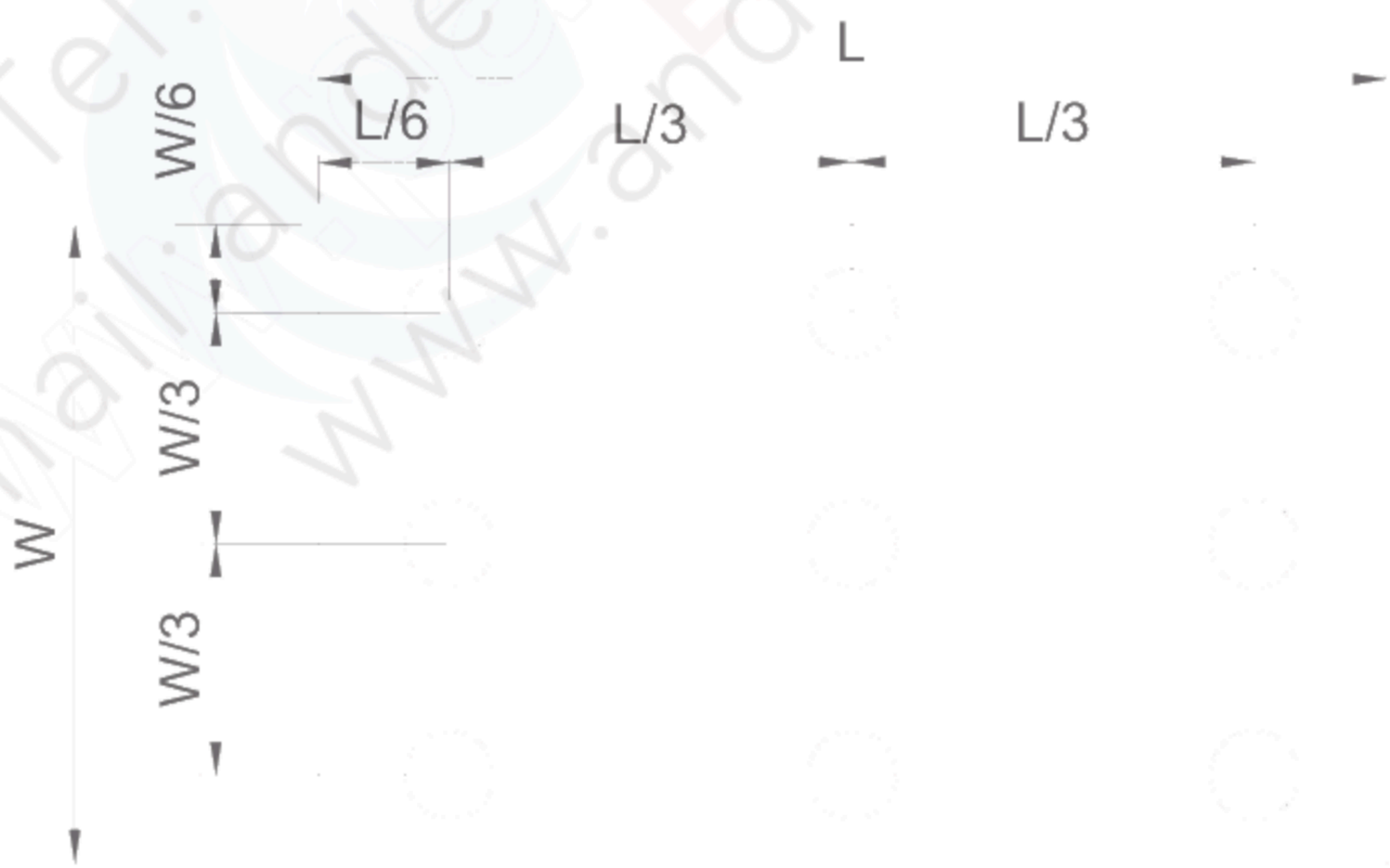


Fig. 4-4 Definition of measuring points

B_{max}: The measured maximum luminance of all measurement position.
B_{min}: The measured minimum luminance of all measurement position.

5. Reliability Test Items

(Note3)

Item	Test Conditions		Remark
High Temperature Storage	Ta = 60℃	240hrs	Note 1，Note 4
Low Temperature Storage	Ta = -20℃	240hrs	Note 1，Note 4
High Temperature Operation	Ts = 50℃	240hrs	Note 2，Note 4
Low Temperature Operation	Ta = -10℃	240hrs	Note 1，Note 4
Operate at High Temperature and Humidity	+40℃, 90%RH	240hrs	Note 4
Thermal Shock	[(-20℃ 30min)→(60℃ 30min)]/cycle，(Ramp ≧20℃/min), 100cycles		Note 4
Package Vibration Test	Random Vibration : ISTA-3A 1Hz~200Hz,Grms=0.53 Half hours for direction of Z		
Package Drop Test	Height:60 cm 1 corner, 3 edges, 6 surfaces		

Note 1: Ta is the ambient temperature of samples.
Note 2: Ts is the temperature of panel's surface.
Note 3: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.
Note 4: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

6. General Precautions

6.1. Safety

Liquid crystal is poisonous. Do not put it in your mouth. If liquid crystal touches your skin or clothes, wash it off immediately by using soap and water.

6.2. Handling

1. The LCD panel is plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
2. The polarizer attached to the display is easily damaged. Please handle it carefully to avoid scratch or other damages.
3. To avoid contamination on the display surface, do not touch the module surface with bare hands.
4. Keep a space so that the LCD panels do not touch other components.
5. Put cover board such as acrylic board on the surface of LCD panel to protect panel from damages.
6. Transparent electrodes may be disconnected if you use the LCD panel under environmental conditions where the condensation of dew occurs.
7. Do not leave module in direct sunlight to avoid malfunction of the ICs.

6.3. Static Electricity

1. Be sure to ground module before turning on power or operating module.
2. Do not apply voltage which exceeds the absolute maximum rating value.

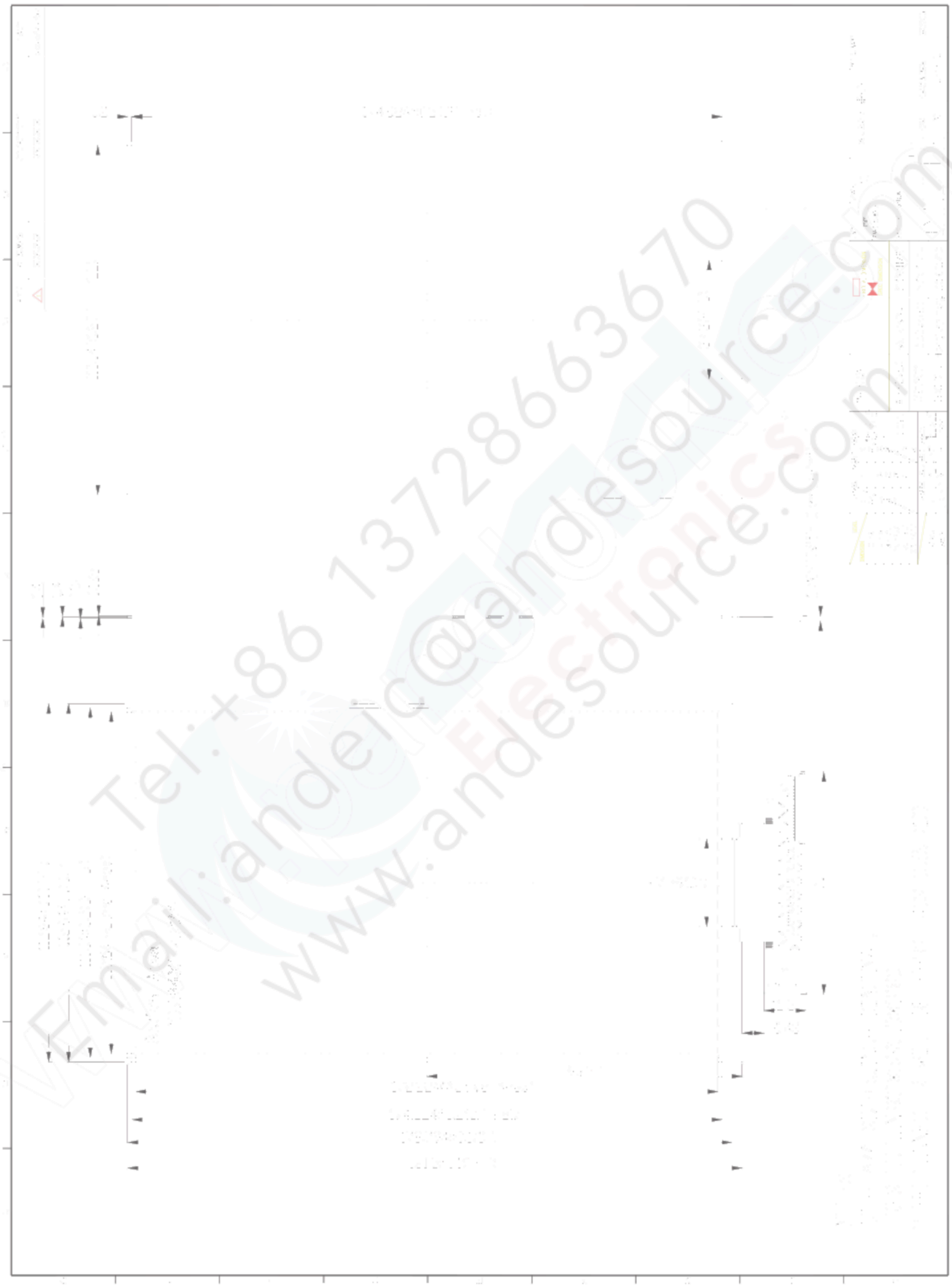
6.4. Storage

1. Store the module in a dark room where must keep at 25±10℃ and 65%RH or less.
2. Do not store the module in surroundings containing organic solvent or corrosive gas.
3. Store the module in an anti-electrostatic container or bag.

6.5. Cleaning

1. Do not wipe the polarizer with dry cloth. It might cause scratch.
2. Only use a soft sloth with IPA to wipe the polarizer, other chemicals might permanent damage to the polarizer.

7. Mechanical Drawing



8. Package Drawing

8.1. Package Material Table

No.	Item	Model (Material)	Dimensions(mm)	Unit Weight (kg)	Quantity	Remark
1	Panel Assembly	TBD	112.64 × 181.80 × 1.07	TBD	TBD	
2	Tray	PET	TBD	TBD	TBD	Anti-static
3	Partition	BC Corrugated Paper	TBD	TBD	TBD	
4	Dust-Proof Bag	PE	TBD	TBD	TBD	
5	Carton	Corrugated paper	TBD	TBD	TBD	
6	Total weight	TBD kg±5%				

8.2. Package Quantity

(1) FOG quantity per PET-Tray:	TBD
(2) Total FOG quantity in Carton:	TBD

8.3. Package Drawing

TBD