PREPARED BY K. Toyota APPROVED BY H. Yabuuchi	SHARP MOBILE LIQUID CRYSTAL DISPLAY GROUP SHARP CORPORATION **SPECIFICATION**	SPEC No. LD-20302A FILE No. ISSUE Apr.3.2008 PAGE Pages 28 APPLICABLE DIVISION MOBILE LCD DIVISION III MOBILE LCD GROUP

DEVICE SPECIFICATION for

TFT LCD Module

(320 × RGB × 240 dots)

Model No.

LQ035Q3DW02

These parts have corresponded with the RoHS directive.

CUSTOMER'S APPROVAL

DATE _____

BY _____

PRESENTED

BY K. Shiono

K. SHIONO
Department General manager
Engineering Department
Mobile LCD Division 3
Mobile Liquid Crystal Display Group
SHARP CORPORATION

RECORDS OF REVISION

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	NO.	PAGE	SUMMARY	NOTE
2008. 04. 03		-	-	1^{st} Issue

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1. Applicable Scope

This specification is applicable to TFT-LCD Module “LQ035Q3DW02”.

2. General Description

This module is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver IC, Input FPC, a back light unit.

Graphics and texts can be displayed on a 320 × RGB × 240 dots panel with about 262k colors by supplying 18bit data signals (6bit × RGB), four timing signals, 3wires 9 / 24bit serial interface signals, logic (Typ. +3.3V),analog (Typ. +3.3V) supply voltages for TFT-LCD panel driving and supply voltage for back light.

3. Mechanical (Physical) Specifications

Item	Specifications	Unit
Screen size	8.8(3.5” type) diagonal	cm
Active area	70.56 (H) × 52.92 (V)	mm
Pixel format	320 (H) × 240 (V)	pixel
	1 Pixel = R+G+B dots	-
Pixel pitch	0.2205 (H) × 0.2205(V)	mm
Pixel configuration	R,G,B vertical stripes	-
Display mode	Normally black	-
Unit outline dimensions *	76.9(W) × 63.9 (H) × Max3.5(D)	mm
Mass	Approx.33	g
Surface treatment	Anti glare	-

*The above-mentioned table indicates module sizes without some projections and FPC.
For detailed measurements and tolerances, please refer to 17. Outline Dimensions.

4. Input Terminal Names and Functions

Recommendation CN：[HIROSE] FH26G-67S-0.3SHBW(05)

Pin No.	Symbol	I/O	Description	Remarks
1	LED_C (-)	-	Power supply for LED (Cathode: Low voltage)	
2	LED_A(+)	-	Power supply for LED (Anode: High voltage)	
3	DGND1	-	Digital Ground	
4	NC	-	Not connected	
5	NC	-	Not connected	
6	NC	-	Not connected	
7	NC	-	Not connected	
8	AGND1	-	Analog Ground	
9	V_{GH}	-	Connect to a Stabilizing capacitor	Note 3
10	C2P	-	Connect a Booster capacitor to C2N	Note 2
11	C2N	-	Connect a Booster capacitor to C2P	
12	C1P	-	Connect a Booster capacitor to C1N	
13	C1N	-	Connect a Booster capacitor to C1P	
14	V_{GL}	-	Connect a Stabilizing capacitor to GND	Note 3
15	C3N	-	Connect a Booster capacitor to C3P	Note 2
16	C3P	-	Connect a Booster capacitor to C3N	
17	AGND2	-	Analog Ground	
18	V_{CIX2}	-	Connect a Stabilizing capacitor to GND	Note 3
19	CYP	-	Connect a Booster capacitor to CYN	Note 2
20	CYN	-	Connect a Booster capacitor to CYP	
21	V_{CI}	-	Booster input voltage pin	Note 3
22	SDO	O	Data output pin in serial mode	
23	AGND3	-	Analog Ground	
24	V_{CIM}	-	Connect a Stabilizing capacitor to GND	Note 3
25	CXP	-	Connect a Booster capacitor to CXN	Note 2
26	CXN	-	Connect a Booster capacitor to CXP	
27	ID	O	ID	Note 1
28	RESB	I	System reset	
29	DGND2	-	Digital Ground	
30	V_{DDIO}	-	Voltage input pin for logic I/O	
31	V_{CORE}	-	Connect a Stabilizing capacitor to GND	Note 3
32	DGND3	-	Digital Ground	
33	SHUT	I	Sleep mode control	
34	CSB	I	Chip select pin of serial interface	
35	SDI	I	Data input pin of serial interface	
36	SCK	I	Clock input pin of serial interface	
37	STYPE	I	9bit / 24bit select pin of serial interface	‘L’=24bit / ‘H’=9bit
38	DEN	I	Display enable signal	
39	B5	I	BLUE data signal(MSB)	
40	B4	I	BLUE data signal	
41	B3	I	BLUE data signal	

Pin No.	Symbol	I/O	Description	Remarks
42	B2	I	BLUE data signal	
43	B1	I	BLUE data signal	
44	B0	I	BLUE data signal(LSB)	
45	G5	I	GREEN data signal(MSB)	
46	G4	I	GREEN data signal	
47	G3	I	GREEN data signal	
48	G2	I	GREEN data signal	
49	G1	I	GREEN data signal	
50	G0	I	GREEN data signal(LSB)	
51	R5	I	RED data signal(MSB)	
52	R4	I	RED data signal	
53	R3	I	RED data signal	
54	R2	I	RED data signal	
55	R1	I	RED data signal	
56	R0	I	RED data signal(LSB)	
57	VSYNC	I	Frame synchronization signal	
58	HSYNC	I	Line synchronization signal	
59	DOTCLK	I	Dot-clock signal	
60	CDUM0	-	Connect a Charge sharing capacitor to GND	Note 4
61	DGND4	-	Digital Ground	
62	V_{LCD63}	-	Connect a Stabilizing capacitor to GND	Note 3
63	V_{COMH}	-	Connect a Stabilizing capacitor to GND	
64	V_{COML}	-	Connect a Stabilizing capacitor to GND	
65	DGND5	-	Digital Ground	
66	CSVCMP	-	Connect a Charge sharing capacitor to CSVCMN	Note 4
67	CSVCMN	-	Connect a Charge sharing capacitor to CSVCMP	

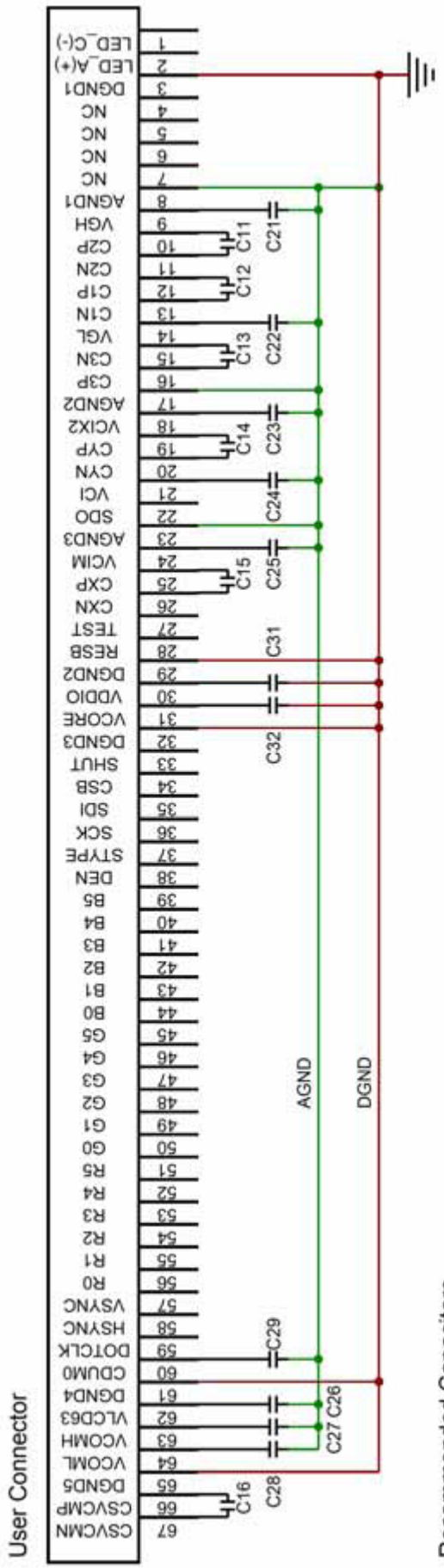
Note 1) ID pin connects with VDDIO on an FPC.

Note 2) Booster Capacitors.

Note 3) Stabilization and charge sharing Capacitors.

Note 4) Charge sharing Capacitors

External recommended condenser



Recommended Capacitors

Ref No.	Capacitance	Rated Voltage	Temperature Characteristic
C11	0.22 µF	16 V	B (JIS) or X5R (EIA)
C12	0.22 µF	16 V	B (JIS) or X5R (EIA)
C13	0.22 µF	16 V	B (JIS) or X5R (EIA)
C14	0.22 µF	10 V	B (JIS) or X5R (EIA)
C15	0.22 µF	6.3 V	B (JIS) or X5R (EIA)
C16	2.2 µF	6.3 V	B (JIS) or X5R (EIA)
C21	2.2 µF	25 V	B (JIS) or X5R (EIA)
C22	2.2 µF	16 V	B (JIS) or X5R (EIA)
C23	2.2 µF	10 V	B (JIS) or X5R (EIA)
C24	2.2 µF	6.3 V	B (JIS) or X5R (EIA)
C25	2.2 µF	6.3 V	B (JIS) or X5R (EIA)
C26	2.2 µF	10 V	B (JIS) or X5R (EIA)
C27	2.2 µF	6.3 V	B (JIS) or X5R (EIA)
C28	2.2 µF	6.3 V	B (JIS) or X5R (EIA)
C29	2.2 µF	6.3 V	B (JIS) or X5R (EIA)
C31	2.2 µF	6.3 V	B (JIS) or X5R (EIA)
C32	2.2 µF	6.3 V	B (JIS) or X5R (EIA)

[Note]
C1N/P, C2N/P, C3N/P, CXN/P, CYN/P are high voltage switching lines on FPC.
Surround/shield by AGND to avoid noise coupling to other pins.
Also aware the PCB design to avoid other components to be affected by noise on those dcdc pins.

5. Absolute Maximum Ratings

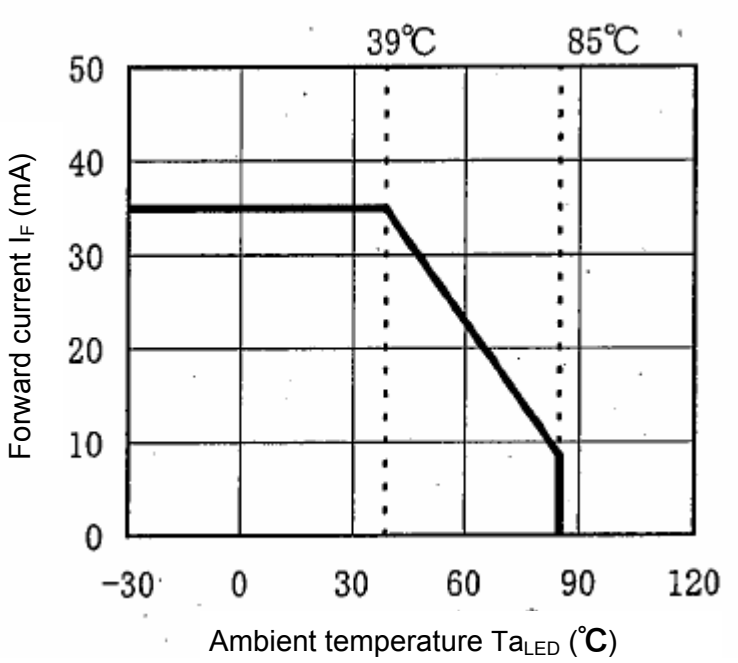
Item	Symbol	Conditions	Rated value	Unit	Remarks
Input voltage	VI	Ta = 25°C	-0.3 ~ V_{DDIO}+0.3	V	Note 1
Logic I/O power supply voltage	V_{DDIO}	Ta = 25°C	-0.3 ~ +4.0	V	
Analog power supply voltage	V_{CI}	Ta = 25°C	AGND-0.3 ~ +5.0	V	
Temperature for storage	Tstg	-	-25 ~ +70	°C	Note 2
Temperature for operation	Topp	-	-10 ~ +70	°C	Note 3
LED input electric current	I_{LED}	Ta = 25°C	35	mA	
LED electricity consumption	P_{LED}	Ta = 25°C	123	mW	Note 4

Note 1) RESB, SHUT, CSB, SDI, SCK, STYPE, DEN, B5~B0, G5~G0, R5~R0, VSYNC, HSYNC, DOTCLK

Note 2) Humidity: 95%RH Max. (Ta≦40°C)
Maximum bulb temperature under 39°C (Ta>40°C) See to it that no dew will be condensed.

Note 3) Panel surface temperature prescribes.

Note 4) Power consumption of one LED (Ta_{LED} = 25°C). (use 7 pieces LED)
Ambient temperature and the maximum input are fulfilling the following operating conditions.



Ambient temperature of LED and the maximum input

6. Electrical Characteristics

6-1. TFT LCD Panel Driving

Ta = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Logic I/O power supply	DC voltage	V_{DDIO}	+3.0	+3.3	+3.6	V	
	DC Current	I_{VDDIO}	-	0.55	0.95	mA	Note 1
Analog power supply	DC voltage	V_{CI}	+3.0	+3.3	+3.6	V	
	DC Current	I_{VCI}	-	9.5	12	mA	Note 1
Permissive input Ripple voltage		$V_{RFVDDIO}$	-	-	100	mVp-p	Note 2
		V_{RFVCI}	-	-	100	mVp-p	Note 2
Logic Input Voltage	High	V_{IH}	0.8 V_{DDIO}	-	V_{DDIO}	V	Note 3
	Low	V_{IL}	0	-	0.2 V_{DDIO}	V	Note 3
Logic input Current		I_{IH} / I_{IL}	-1	-	1	μA	Note 3

Note 1) V_{DDIO} = V_{CI} = +3.3V
Current situation for I_{VDDIO}: Black & White checker flag pattern
Current situation for I_{CI}: All white pattern

Note 2) V_{DDIO} = V_{CI} = +3.3V

Note 3) RESB, SHUT, CSB, SDI, SCK, STYPE, DEN, B5~B0, G5~G0, R5~R0, VSYNC, HSYNC, DOTCLK

6-2. Power up sequence

V_{DDIO} / V_{CI} ON (hold RESB = “L”)

↓

Wait min. 80us

↓

Hard Reset (RESB “L” → “H”)

↓

Display Data Start (VSYNC, HSYNC, DOTCLK)

↓

Enter the Sleep Mode

Reg. #	Register	Data	Remark
R11h	Power control (8)	0001 h	Note 2

↓

Register setting

Reg. #	Register	Data (Gamma 2.2)	Remark
R01 h	Driver output control	0xEF h	Note 1
R02 h	LCD drive AC control	0300h	
R03 h	Power control (1)	0A0E h	
R0B h	Frame cycle control	D000 h	
R0C h	Power control (2)	0005 h	
R0D h	Power control (3)	000F h	
R0E h	Power control (4)	2E00 h	
R12 h	Input data format	006x h	Note 3
R16 h	Horizontal Porch	9F86 h	Note 4
R17 h	Vertical Porch	0002 h	Note 5
R1E h	Power control (5)	0000 h	
R28 h	Power control (6)	0006 h	
R2A h	Power control (7)	0187 h	
R30 h	Gamma control (1)	0006 h	
R31 h	Gamma control (2)	0207 h	
R32 h	Gamma control (3)	0000 h	
R33 h	Gamma control (4)	0107 h	
R34 h	Gamma control (5)	0707 h	
R35 h	Gamma control (6)	0005 h	
R36 h	Gamma control (7)	0107 h	
R37 h	Gamma control (8)	0707 h	
R3A h	Gamma control (9)	1F00 h	
R3B h	Gamma control (10)	0000 h	

↓

Exit the Sleep Mode

Reg. #	Register	Data	Remark
R11h	Power control (8)	0000 h	

↓

Wait 10 frames time

↓

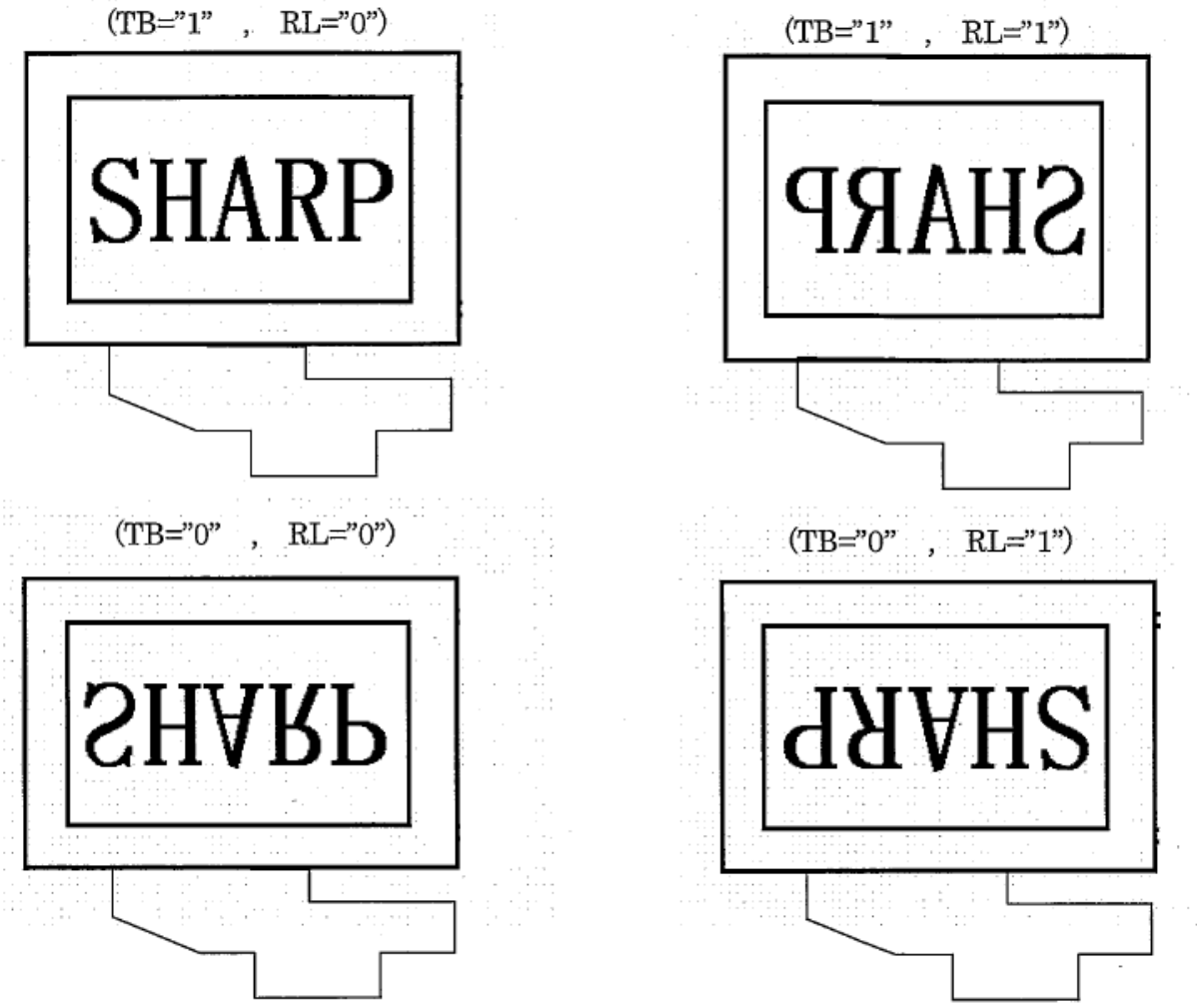
Display On

Note 1)

Driver Output Control (R01h)(POR=0xEFh)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	1	0	TB	RL	1	1	1	0	1	1	1	1
POR		0	0	0	0	1	0	x	x	1	1	1	0	1	1	1	1

≪Vertical and Horizontal inversion function(TB, RL)≫



Note 2)

mode Control (R11h)(POR=0x0x h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	CM	0	0	0	0	0	0	0	SHUT
POR		0	0	0	0	0	0	0	x	0	0	0	0	0	0	0	x

CM : CM = “0”, 262K-color mode. CM = “1”, 8 color mode.

SHUT : SHUT =”0”, normal mode. SHUT =”1”, sleep mode.

Note 3)

mode Control (R12h)(POR=006x h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	IF1	IF0	CM1	IFS1	IFS0	0	0
POR		0	0	0	0	0	0	0	0	0	1	1	0	0	x	0	0

R12h	DEN mode	HV SYNC mode
0060h	Yes	No
0064h	No	Yes

In the case of a DEN mode, more than Vertical Porch = 2 and Horizontal Porch = 4.

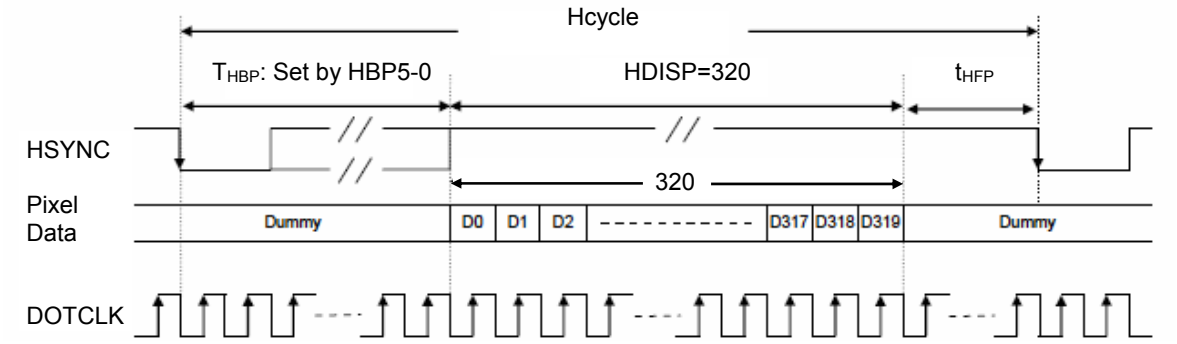
Note 4)

Horizontal Porch(R16h)(POR=9F86h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	1	0	0	1	1	1	1	1	1	0	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
POR		1	0	0	1	1	1	1	1	1	0	0	0	0	1	1	0

HBP5-0: Set the delay period from falling edge of HSYNC to first valid line.

HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	No. of clock cycle of DOTCLK
0	0	0	0	0	0	2
0	0	0	0	0	1	3
0	0	0	0	1	0	4
0	0	0	0	1	1	5
0	0	0	1	0	0	6
:	:	:	:	:	:	: Step = 1 :
1	1	1	1	1	0	64
1	1	1	1	1	1	65



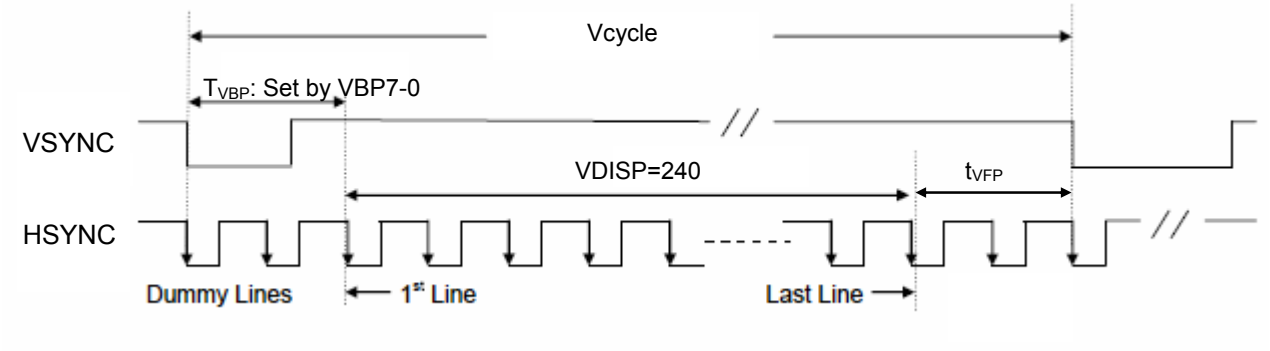
Note 5)

Vertical Porch(R17h)(POR=0002h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

VBP8-0 : Set the delay period from falling edge of VSYNC to first valid line.

VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
:	:	:	:	:	:	:	:	: Step = 1 :
1	1	1	0	1	1	1	1	239
1	1	1	1	0	0	0	0	240
1	1	1	1	*	*	*	*	Reserved



6-3. Power down sequence

Write White Data (RGB Data: All “H” level)

↓

Wait min. 1 frame time

↓

Enter the Sleep Mode

Reg. #	Register	Data	Remark
R11h	Power control (8)	0001 h	

↓

Wait min. 2 frames time

↓

Display Data Stop (VSYNC, HSYNC, DOTCLK)

↓

V_{DDIO} / V_{CI} OFF

6-3. Back light driving

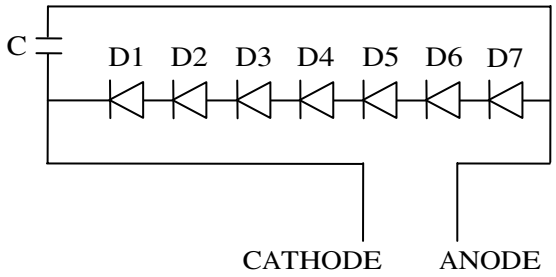
The back light system has 7 LEDs

Used LED : NSSW006T[NICHIA] [Luminance: A18～A22 , Chromaticity:a62,a67,bj2,bj7]

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Rated Voltage	V_{BL}	-	22.4	24.5	V	
Rated Current	I_L	-	20	-	mA	Ta=25°C
Power consumption	W_L	-	448	-	mW	

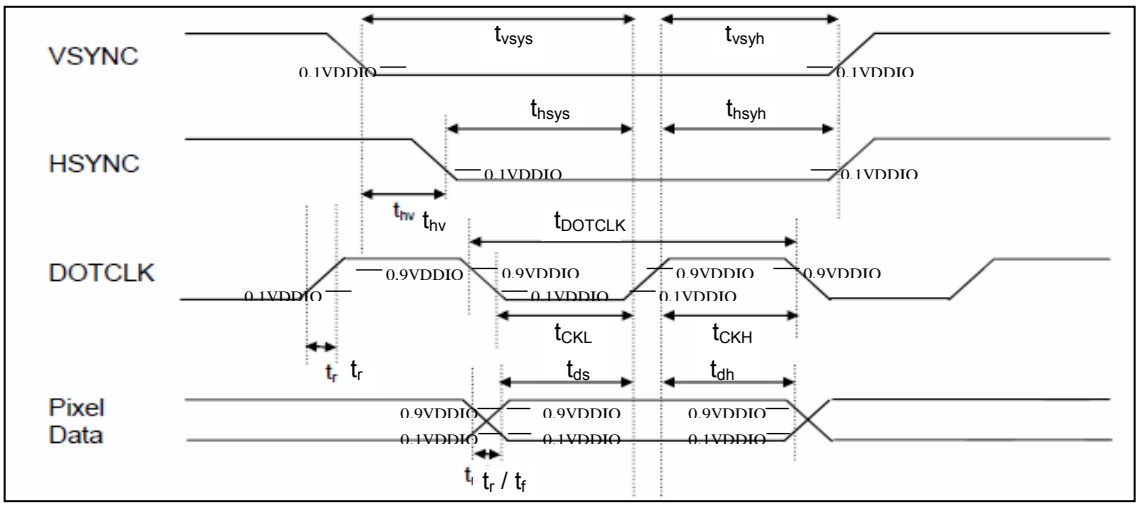
[LED-FPC circuit]

Capacitor:
0.1uF / 35V
or
4700pF / 50V



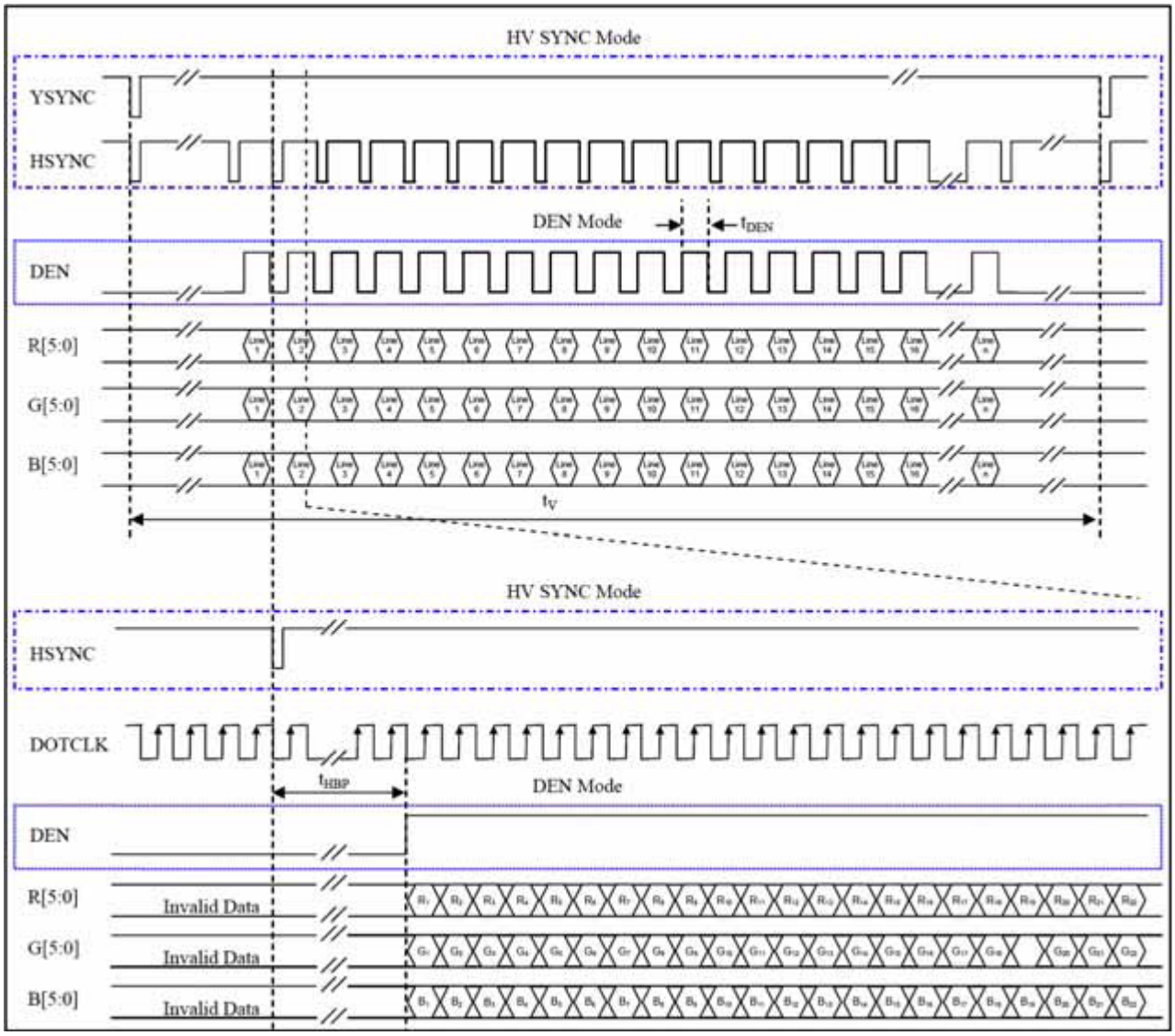
7. Timing characteristics of input signals

7-1. Pixel Clock Timing



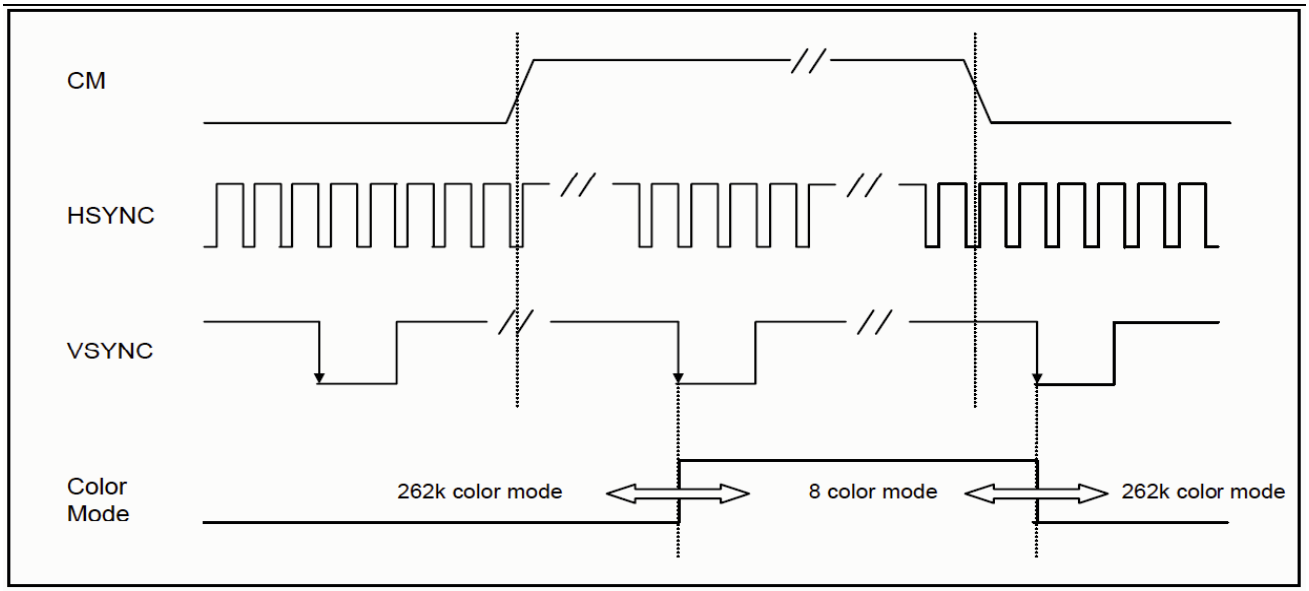
Characteristics		Symbol	Min	Typ	Max	Unit
DOTCLK	Frequency	f_{DOTCLK}	-	5.0	8.0	MHz
	Period	t_{DOTCLK}	125	200	-	nSec
	High Period	t_{CKH}	16	-	-	nSec
	Low Period	t_{CKL}	16	-	-	nSec
Data	Setup Time	t_{ds}	10	-	-	nSec
	Hold Time	t_{dh}	10	-	-	nSec
Vsync	Setup Time	t_{vsys}	5	-	-	nSec
	Hold Time	t_{vsyh}	5	-	-	nSec
Hsync	Setup Time	t_{hsys}	5	-	-	nSec
	Hold Time	t_{hsyh}	5	-	-	nSec
Phase difference of Sync signal Falling edge		t_{hv}	0	-	320	t_{DOTCLK}
Reset Pulse Width		t_{RES}	2.5	-	-	nSec
Rise / Fall Time		t_r/t_f	5	-	25	nSec

7-2. Data Transaction Timing in Normal Operating Mode (262k color)

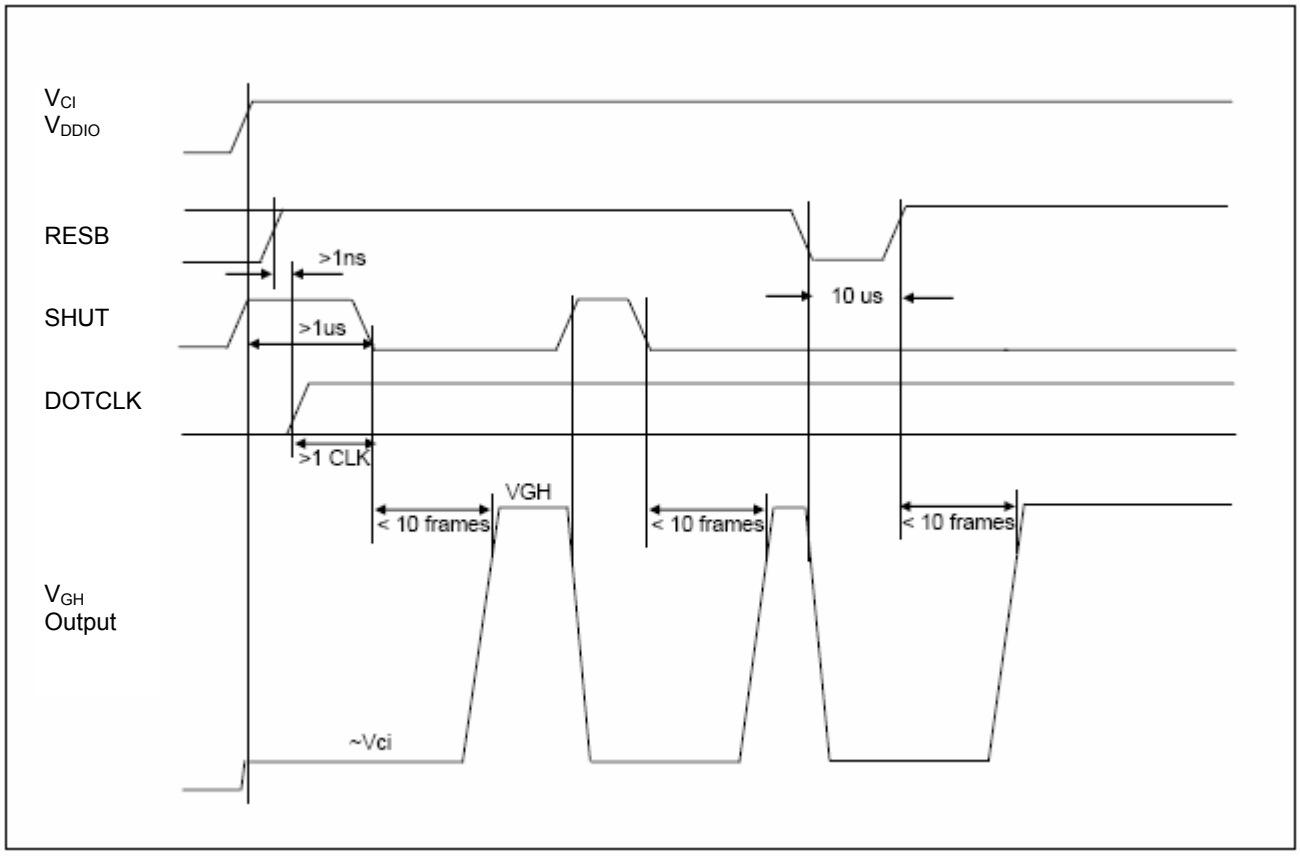


Characteristics		Symbol	HV SYNC MODE	DEN MODE	Unit
DOTCLK Frequency		$1/t_{DOTCLK}$	5	5	MHz
HSYNC	Period	t_H	336	336	t_{DOTCLK}
	Horizontal Display Area	t_{data}	320	320	t_{DOTCLK}
	Horizontal Back Porch	t_{HBP}	8	-	t_{DOTCLK}
	Horizontal Front Porch	t_{HFP}	8	-	t_{DOTCLK}
	Data Enable Period	t_{DEN}	-	320	t_{DOTCLK}
VSYNC	Period	t_V	244	244	t_H
	Vertical Display Area	t_{AL}	240	240	t_H
	Vertical Back Porch	t_{VBP}	2	-	t_H
	Vertical Front Porch	t_{VFP}	2	-	t_H

7-3. Synchronization Signals Timing in Power Save Mode (8 color)



7-4. V_{GH} Output against SHUT & RESB



VGH Output against SHUT & RESB

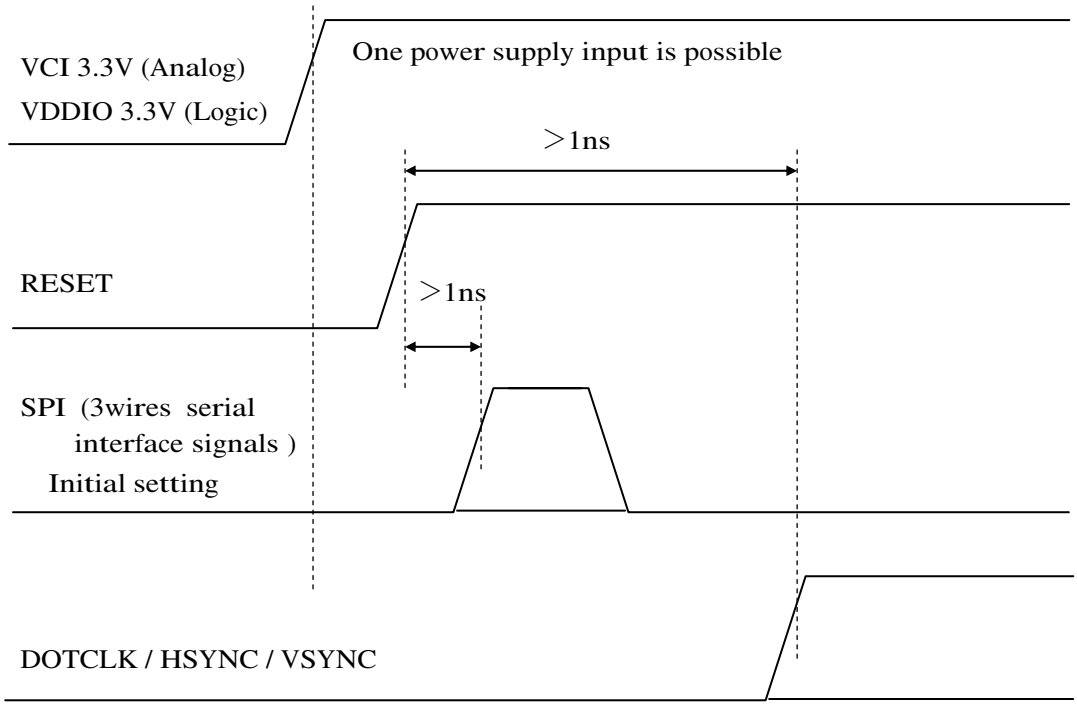
Note1: The minimum cycle time of SHUT is 10 + 2 frames.

Note2: DOTCLK must be provided for boosting of V_{GH}. The above timing diagram assumed voltages and DOTCLK are continuous supplied after power on.

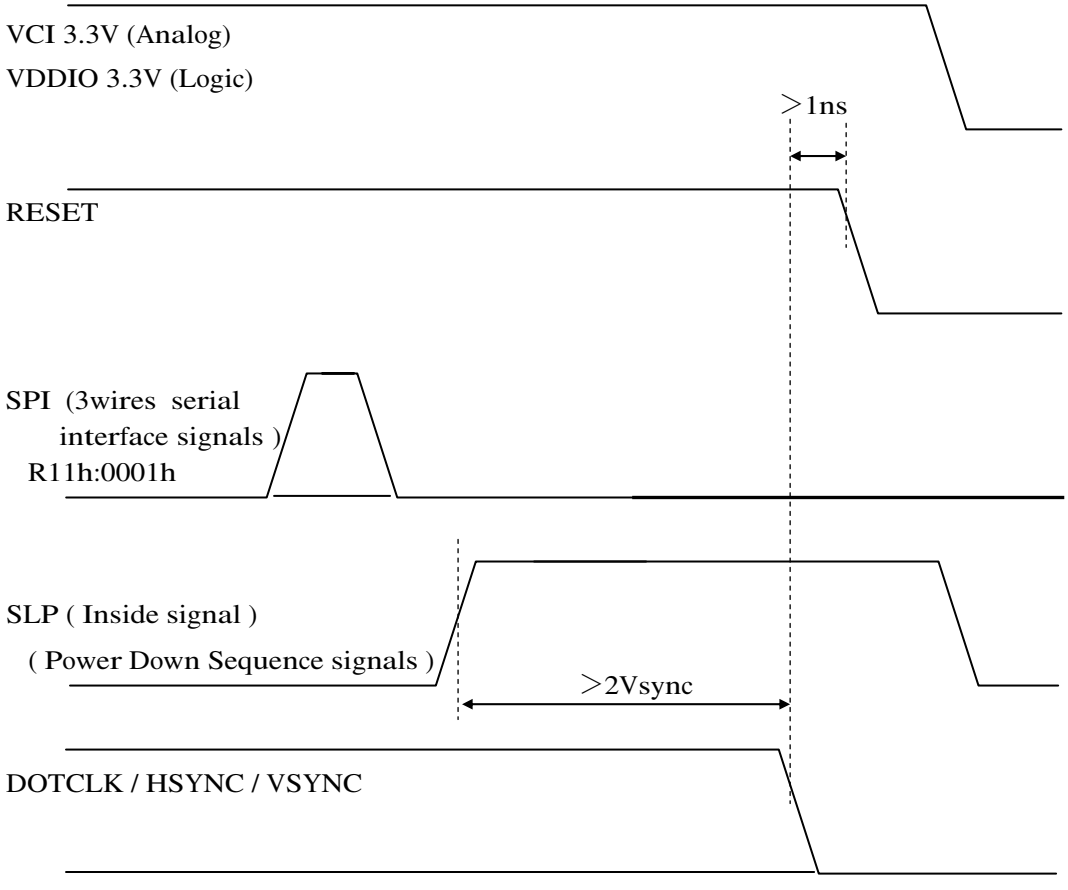
Note3: V_{GH} will be forced to V_{CI} at the low stage of RESB.

Note4: The minimum pulse width of RESET is 10us.

7-5. Power Up Sequence

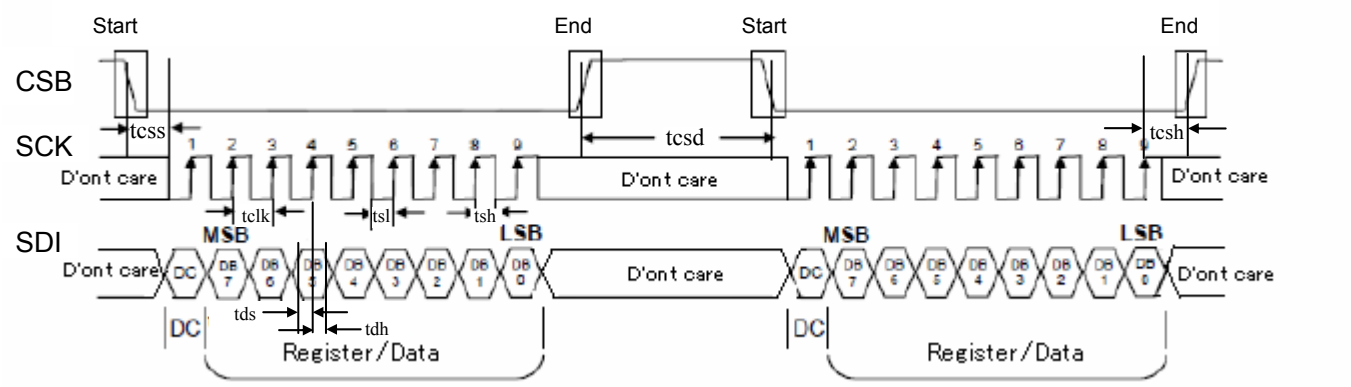


7-6. Power Down Sequence

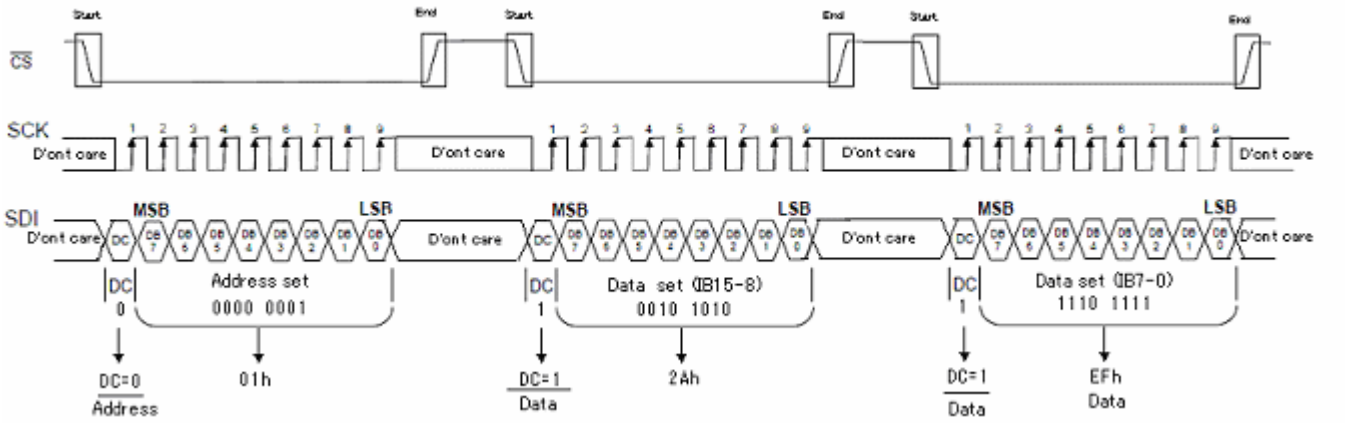


7-7. SPI Interface Timing Diagram & Transaction Example

1) 3wire 9bit



The example transmit “2AEFh” to register R01h.



2) 3wire 24bit

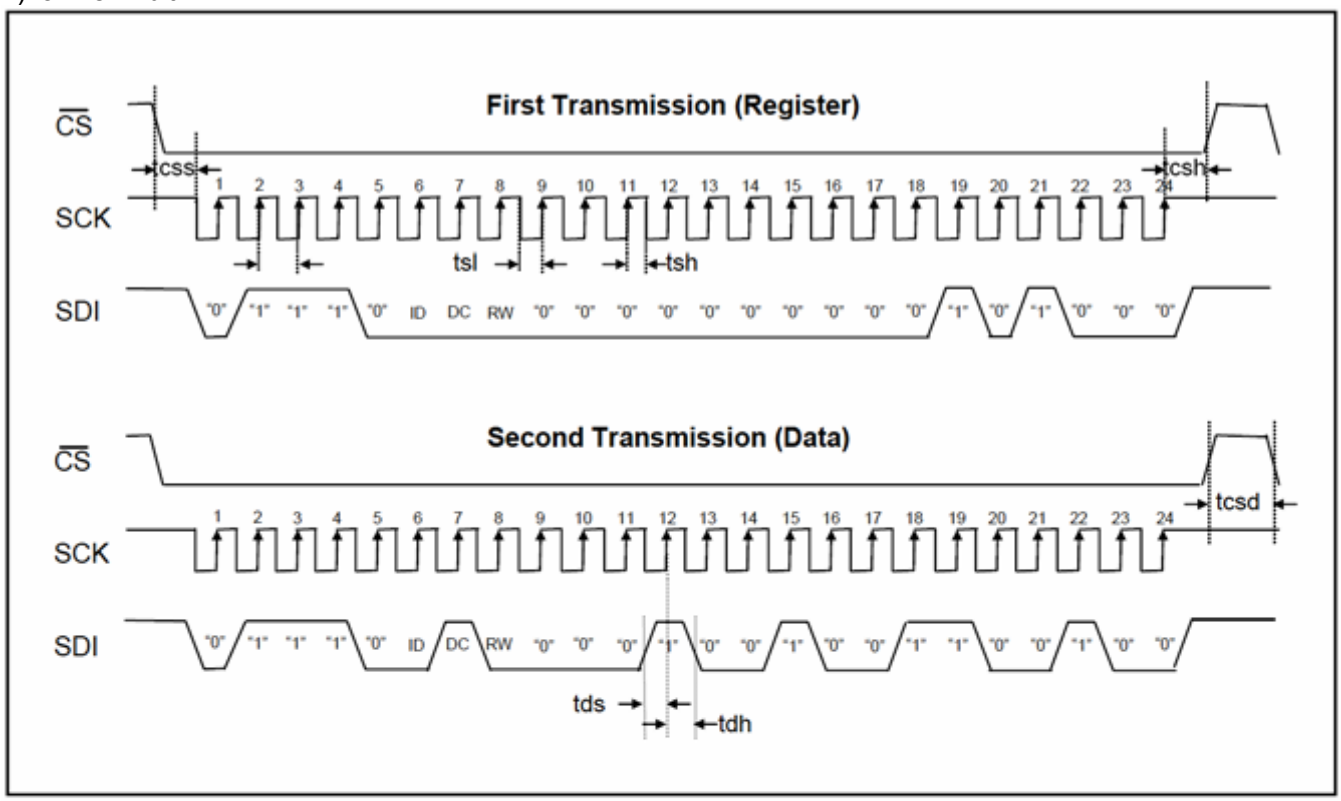
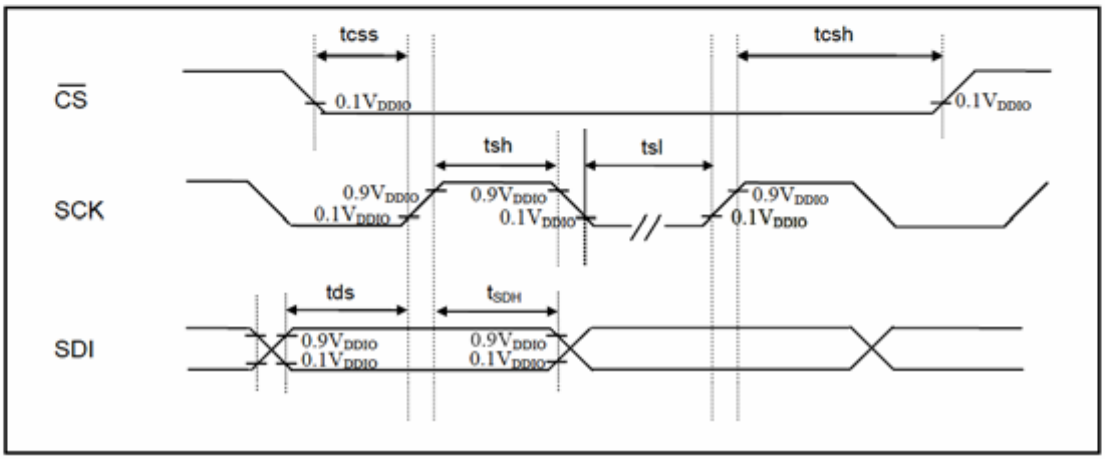
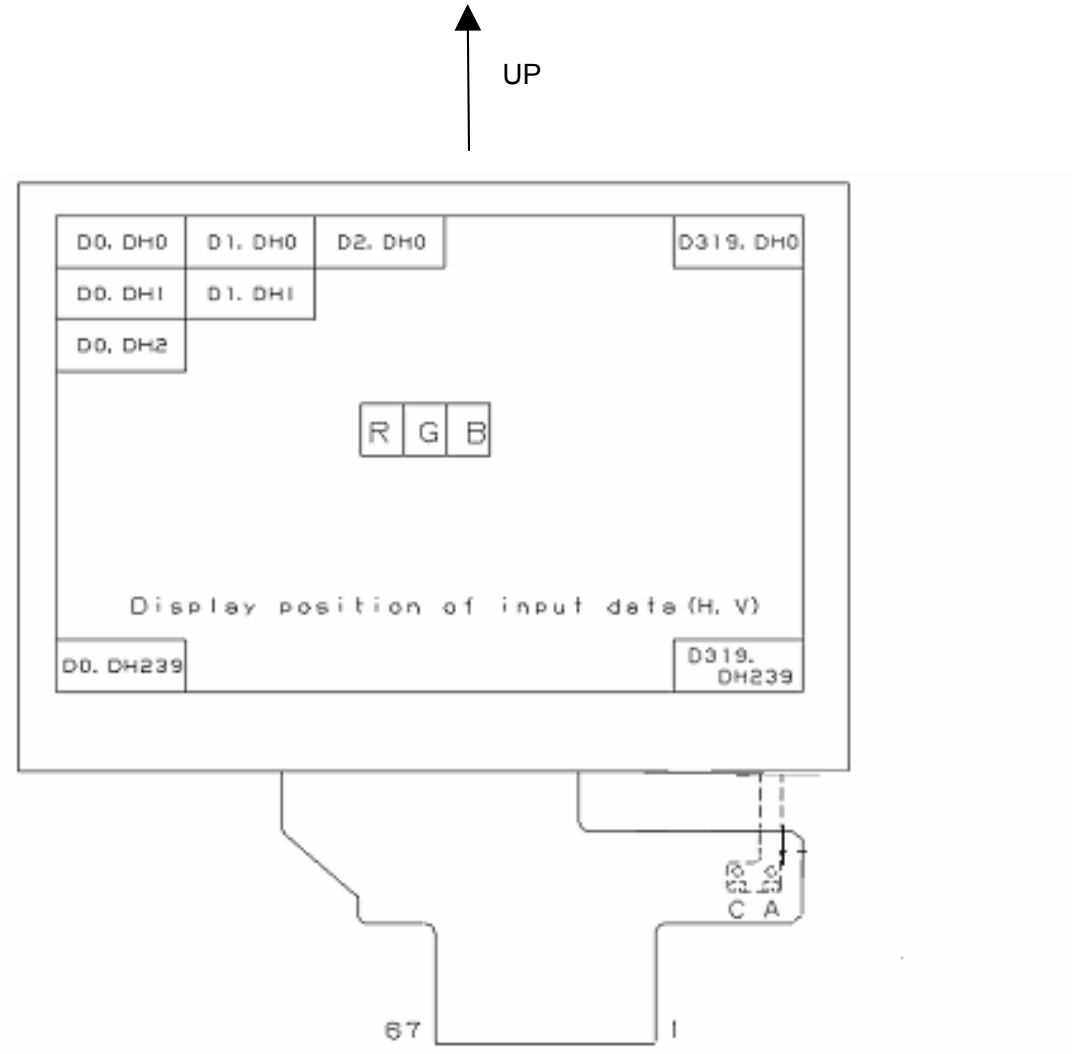


Figure 15-6 - SPI Interface Timing Diagram & Transaction Example



Characteristics		記 号	Min	Typ	Max	単 位
Serial Clock	Frequency	fclk	-	-	20	MHz
	Cycle Time	tclk	50	-	-	ns
	Low Width	tsl	25	-	-	ns
	High Width	tsh	25	-	-	ns
Chip Select	Setup Time	tcss	0	-	-	ns
	Hold time	tcsh	10	-	-	ns
	High Delay Time	tcsd	20	-	-	ns
Data	Setup Time	tds	5	-	-	ns
	Hold Time	tdh	10	-	-	ns

7-8. Input Data Signals and Display Position on the screen



Please refer to 4. Input Terminal Names and Functions

Please refer to 17. Outline Dimensions.

8. Input Signals, Basic Display Colors and Gray Scale of Each Color

	Colors & Gray Scale	Gray Scale	Date signal																	
			R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5
			LSB					MSB	LSB					MSB	LSB					MSB
Basic Color	Black	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	–	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Green	–	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	–	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Red	–	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	–	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	–	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	⇩	GS62	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS63	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
	⇩	GS62	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
	Green	GS63	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1
	⇩	GS62	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	Blue	GS63	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

0: Low level voltage, 1: High level voltage

Each basic color can be displayed in 64 gray scales from 6 bit data signals.
According to the combination of 18 bit data signals, the 262k color display can be achieved on the screen.

9. Optical Characteristics

Ta = 25°C, V_{DDIO} = +3.3V, V_{CI} = +3.3V

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range (Wide View)	Horizontal	θ21	CR≧10	-	80	-	deg.	【Note1,4】
		θ22		-	80	-	deg.	
	Vertical	θ11		-	80	-	deg.	
		θ12		-	80	-	deg.	
Contrast ratio		CR	Optimum viewing angle	100	500	-		【Note2,4】
Response Time	Rise	Tr	θ=0°	-	15	30	ms	【Note3,4】
	Decay	Td		-	15	30	ms	
Chromaticity of White		x		0.26	0.31	0.36	-	【Note4】
		y		0.29	0.34	0.39	-	
Luminance of white		X_{L1}		350	450	-	cd/m²	I_{LED}=20mA 【Note4】

* The optical characteristics measurements are operated under a stable luminescence (I_{LED} = 20mA) and a dark condition. (Refer to Fig.9-1 and Fig.9-2)

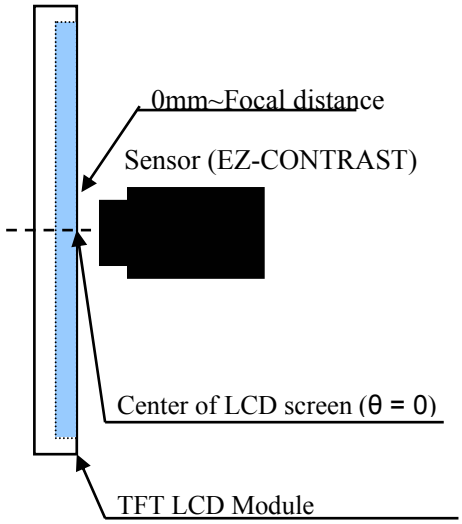


Fig.9-1 Measuring setup for Viewing angle and Response time

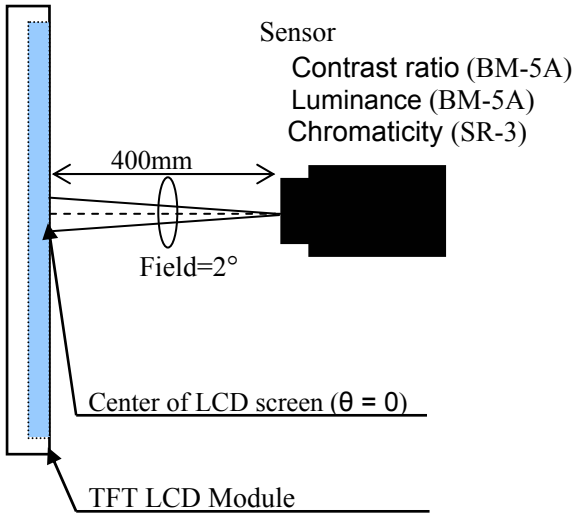
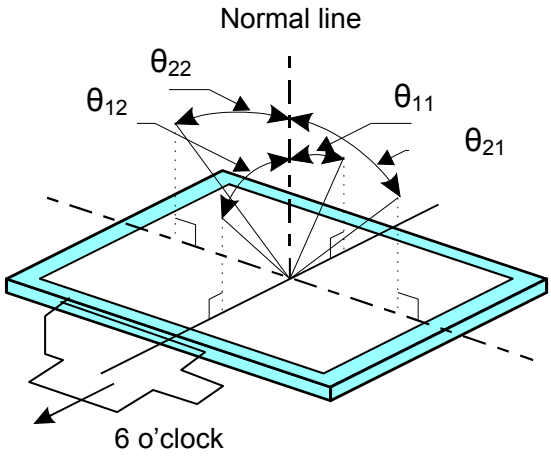


Fig.9-2 Measuring setup for Luminance, Chromaticity and Contrast ratio

【 Note 1 】Definitions of viewing angle range



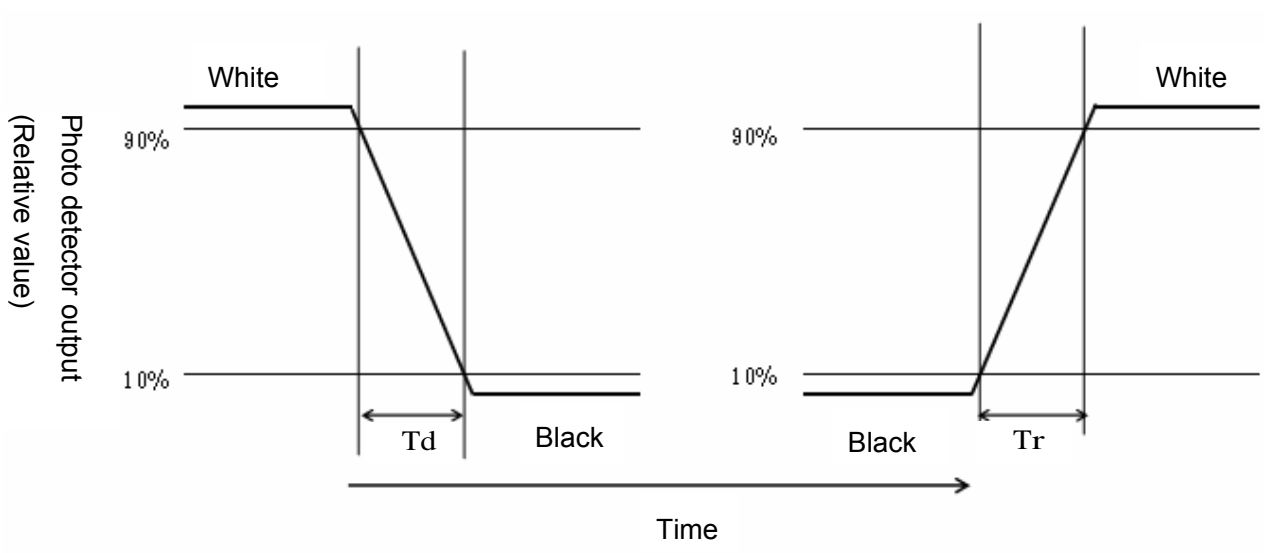
【 Note 2 】Definition of contrast ratio

The contrast ratio is defined as the following

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance (brightness) with all pixels white}}{\text{Luminance (brightness) with all pixels black}}$$

【 Note 3 】Definition of response time

The response time is defined as the following figure and shall be measured by switching the input signal for “Black” and “White”



【 Note 4 】This shall be measured at center of the screen.

10 Handling of modules

10-1. Inserting the FPC into its connector and pulling it out

1) Be sure to turn off the power supply and the signals when inserting or disconnecting the cable.
2) Please insert for too much stress not to join FPC in the case of insertion of FPC.

10-2. About handling of FPC

1) The bending radius of the FPC should be more than 1.4mm, and it should be bent evenly.
2) Do not dangle the LCD module by holding the FPC, or do not give any stress to it.

10-3. Mounting of the module

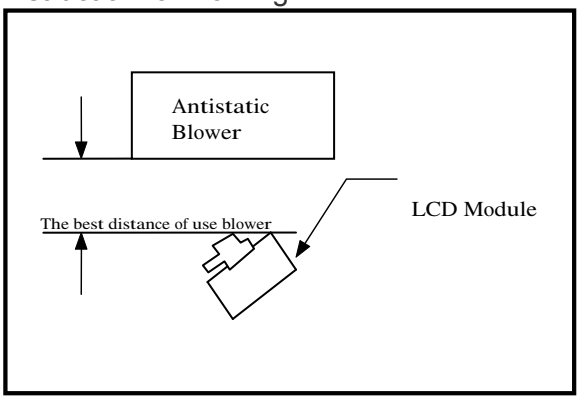
1) The module should be held on to the plain surface. Do not give any warping or twisting stress to the module.
2) Please consider that GND can ground a modular metal portion etc. so that static electricity is not charged to a module.

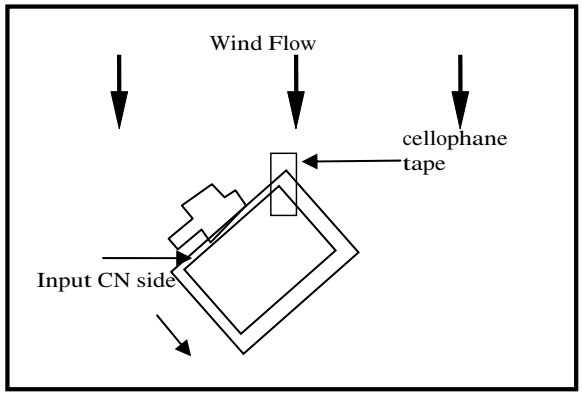
10-4. Cautions in assembly / Handling pre cautions

As the polarizer can be easily scratched, be most careful in handling it.

1) Work environments in assembly.
   Since removing laminator may causes electrostatic charge that tends to attract dust, the following work environment would be desired.
   a) Floor: Conductive treatment having 1MΩ resistance onto floor's tile
   b) The room free from dust coming from outdoor environment, and put an adhesive mat at entrances.
   c) Humidity from 50% to 70% and temperature from 15°C to 27°C are desirable.
   d) Worker should ware conductive shoes, conductive fatigue, conductive glove and earth wrist band.

2) Instruction for working





a) Wind direction of an antistatic blower should slightly downward to properly blow the module. The distance between the blower and the module should be the best distance of use blower. Also, pay attention to the direction of the module.
b) To prevent polarizer from scratching, adhesive tape (cellophane tape) should be stuck at the part of laminator sheet, which is closed to blower. [See the above]
c) Pull slowly adhesive tape to peel the laminator off, with spending more than 5 second.
d) The module without laminator should be moved to the next process to prevent adhesion of dust.

3) How the remove dust on the polarizer

a) Blow out dust by the use of an N2 blower with antistatic measures taken. Use of an ionized air Gun is recommendable.

b) When the panel surface is soiled, wipe it with soft cloth.

4) In the case of the module's metal part (shield case) is stained, wipe it with a piece of dry, soft cloth. If rather difficult, give a breath on the metal part to clean better.

5) If water dropped, etc. remains stuck on the polarizer for a long time, it is apt to get discolored or cause stains. Wipe it immediately.

6) As a glass substrate is used for the TFT-LCD panel, if it is dropped on the floor or hit by something hard, it may be broken or chipped off.

7) Since CMOS LSI is used in this module, take care of static electricity and take the human earth into consideration when handling.

10-5. Others

1) Regarding storage of LCD modules, avoid storing them at direct sunlight-situation.

2) If stored at temperatures below the rated values, the inner liquid crystal may freeze, causing cell destruction. At temperatures exceeding the rated values for storage, the liquid crystal may become isotropic liquid, making it no longer possible to come back to its original state in some cases.

3) If the LCD is broken, do not drink liquid crystal in the mouth. If the liquid crystal adheres to a hand or foot or to clothes, immediately cleanse it with soap.

4) If a water drop or dust adheres to the polarizer, it is apt to cause deterioration. Wipe it immediately.

5) Be sure to observe other caution items for ordinary electronic parts and components.

11. Reliability test items

No.	Test item	Conditions
1	High temperature storage test	Leaves the module at Ta=+70°C for 240h
2	Low temperature storage test	Leaves the module at Ta=-25°C for 240h
3	High temperature & high humidity operation test	Operates the module at Ta=+40°C; 95%RH for 240h (No condensation)
4	High temperature operation test	Operates the module with +70°C at panel surface for 240h
5	Low temperature operation test	Operates the module at Ta=--10°C for 240h
6	Vibration test (non- operating)	Frequency range: 10 to 55Hz Stroke: 1.5mm Sweep time: 1minutes Test period: 2 hours (40 minutes for each direction of X,Y,Z)
7	Shock test	Impact value: 980m/s², Action time 6ms Direction: ±X, ±Y, ±Z, Time: Third for each direction.
8	Thermal shock test	Ta=-25°C to 70°C /10 cycles (30 min) (30min)

【Note】Ta = Ambient temperature, Tp = Panel temperature

【Check items】

In the standard condition, there shall be no practical problems that may affect the display function.

12. Display Grade

The standard regarding the grade of color LCD displaying modules should be based on the delivery inspection standard.

13. Delivery Form

1) Carton piling-up: Max 8 rows

2) Environments

Temperature: 0～40°C

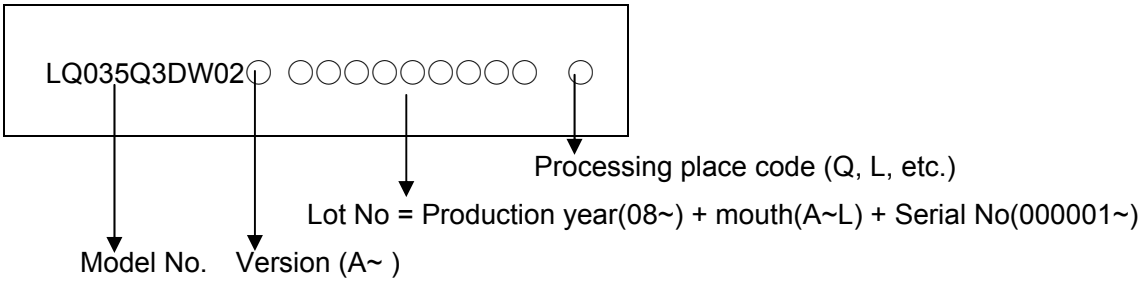
Humidity: 65% RH or less (at 40°C)

There should be no dew condensation even at a low temperature and high humidity.

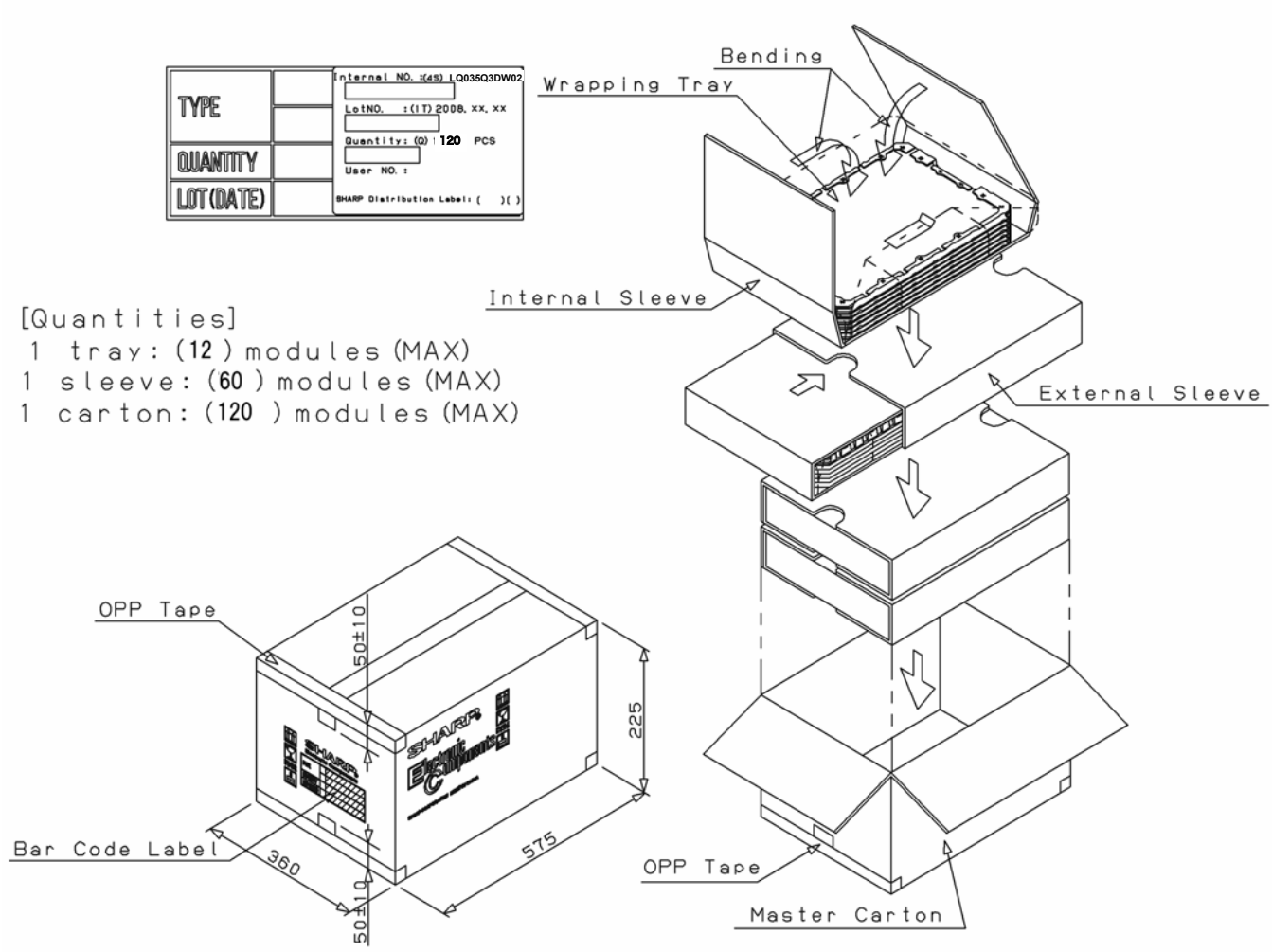
3) Packing form: 15. LCD module packing carton

14. Lot No. marking

The lot No. will be indicated on individual inkjet. The location is as shown



15. LCD module packing carton



16. Others

1 Disassembling the module can cause permanent damage and you should be strictly avoided.

2 Please be careful that you don't keep the screen displayed fixed pattern image for a long time, since retention may occur.

3 If any problem arises regarding the items mentioned in this specification sheet or otherwise, it should be discussed and settled mutually in a good faith for remedy and/or improvement.

17. Outline Dimensions