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SPECIFICATION

DEVICE SPECIFICATION for

TFT LCD Module

(1080× RGB × 1920 dots)

Model No.

LS055T3SX05

☐CUSTOMER'S APPROVAL

DATE _____

BY _____

PRESENTED BY

H.WATATANI

GENERAL MANAGER

DEVELOPMENT DEPT. I DESIGN CENTER I

LCD DESIGN DEVELOPMENT

DISPLAY DEVICE BUSINESS GROUP

SHARP (CHINA) INVESTMENT CO.,LTD.

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[For handling and system design]

(1) Do not scratch the surface of the polarizer film as it is easily damaged.

(2) If the cleaning of the surface of the LCD panel is necessary, wipe it swiftly with cotton or other soft cloth. Do not use organic solvent as it damages polarizer.

(3) Water droplets on polarizer must be wiped off immediately as they may cause color changes, or other defects if remained for a long time.

(4) Since this LCD panel is made of thin glass, dropping the module or banging it against hard objects may cause cracks or fragmentation

(5) Certain materials such as epoxy resin (amine's hardener) or silicone adhesive agent (de-alcohol or de-oxym) emits gas to which polarizer reacts (color change). Check carefully that gas from materials used in system housing or packaging do not hart polarizer.

(6) Liquid crystal material will freeze below specified storage temperature range and it will not get back to normal quality even after temperature comes back within specified temperature range. Liquid crystal material will become isotropic above specified temperature range and may not get back to normal quality. Keep the LCD module always within specified temperature range.

(7) Do not expose LCD module to the direct sunlight or to strong ultraviolet light for long time.
(8) If the LCD driver IC (COG) is exposed to light, normal operation may be impeded. It is necessary to design so that the light is shut off when the LCD module is mounted.

(9) Do not disassemble the LCD module as it may cause permanent damage.

(10) As this LCD module contains components sensitive to electrostatic discharge, be sure to follow the instructions in below.

① Operators

Operators must wear anti-static wears to prevent electrostatic charge up to and discharge from human body.

② Equipment and containers

Process equipment such as conveyer, soldering iron, working bench and containers may possibly generate electrostatic charge up and discharge. Equipment must be grounded through 100Mohms resistance. Use ion blower.

③ Floor

Floor is an important part to leak static electricity which is generated from human body or equipment. There is a possibility that the static electricity is charged to them without leakage in case of insulating floor, so the countermeasure (electrostatic earth: $1\times10^{8}\Omega$) should be made.

④Humidity

Proper humidity of working room may reduce the risk of electrostatic charge up and discharge. Humidity should be kept over 50% all the time.

⑤Transportation/storage

Storage materials must be anti-static to prevent causing electrostatic discharge.

⑥Others

Protective film is attached on the surface of LCD panel to prevent scratches or other damages. When removing this protective film, remove it slowly under proper anti-ESD control such as ion blower.

(11) Hold LCD very carefully when placing LCD module into the system housing. Do not apply excessive stress or pressure to LCD module. Do not to use chloroprene rubber as it may affect on the reliability of the electrical interconnection.

(12) Do not hold or touch LCD panel to flex interconnection area as it may be damaged.

(13) As the binding material between LCD panel and flex connector mentioned in 12) contains an organic material, any type of organic solvents are not allowed to be used. Direct contact by fingers is also prohibited.

(14) When carrying the LCD module, place it on the tray to protect from mechanical damage. It is recommended to use the conductive trays to protect the CMOS components from electrostatic discharge. When holding the module, hold the Plastic Frame of LCD module so that the panel, COG and other electric parts are not damaged.

(15) Do not touch the COG's patterning area. Otherwise the circuit may be damaged.

(16) Do not touch LSI chips as it may cause a trouble in the inner lead connection.

(17) Place a protective cover on the LCD module to protect the glass panel from mechanical damages.

(18) LCD panel is susceptible to mechanical stress and even the slightest stress will cause a color change in background. So make sure the LCD panel is placed on flat plane without any continuous twisting, bending or pushing stress.

(19) Protective film is placed onto the surface of LCD panel when it is shipped from factory. Make sure to peel it off before assembling the LCD module into the system. Be very careful not to damage LCD module by electrostatic discharge when peeling off this protective film. Ion blower and ground strap are recommended.

(20) Make sure the mechanical design of the system in which the LCD module will be assembled matches specified viewing angle of this LCD module.

(21) This LCD module does not contain nor use any ODS (1,1,1-Trichloroethane, CCL4) in all materials used, in all production processes.

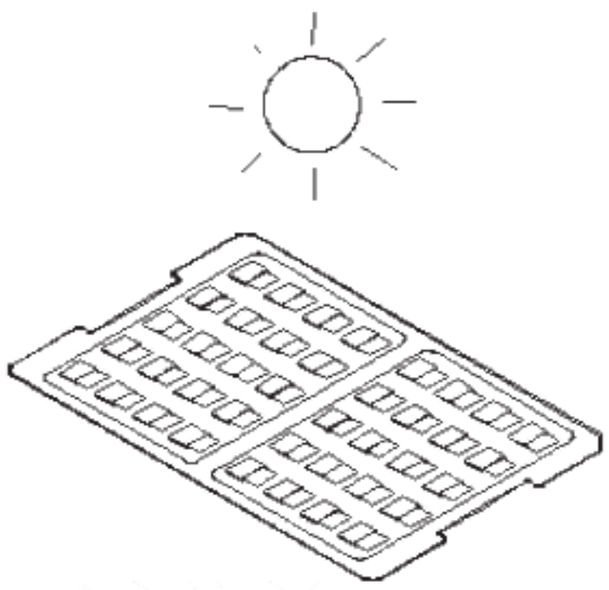
[For operating LCD module]

(1) Do not operate or store the LCD module under outside of specified environmental conditions.
(2) At the shipment, adjust the contrast of each LCD module with electric volume. LCD contrast may vary from panel to panel depending on variation of LCD power voltage from system.
(3) As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable.

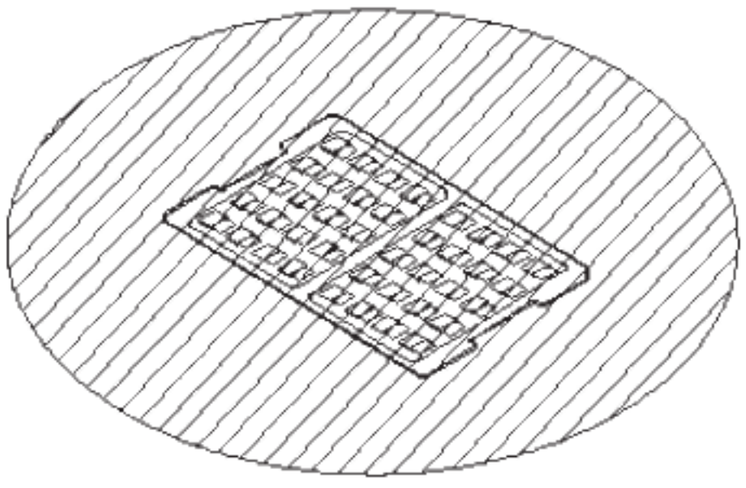
[Precautions for Storage]

(1) Do not expose the LCD module to direct sunlight or strong ultraviolet light for long periods. Store in a dark place.
(2) The liquid crystal material will solidify if stored below the rated storage temperature and will become an isotropic liquid if stored above the rated storage temperature, and may not retain its original properties. Only store the module at normal temperature and humidity (25±5°C,60±10%RH) in order to avoid exposing the front polarizer to chronic humidity.
*Under the condition of long time high temperature storage, module's warpage may happen, so the module should be stored at normal temperature(20±5°C).
*Under the condition of high humidity, module's warpage also may happen, so the module should be immediately stuck with Touch panel after being opened from the degas package. Otherwise don't store the module at the high humidity condition.
(3) Keeping Method
a. Don't keeping under the direct sunlight.
b. Keeping in the tray under the dark place.

DON'T



DO



(4) Do not operate or store the LCD module under outside of specified environmental conditions.
(5) Be sure to prevent light striking the chip surface.

[Other Notice]

(1) Do not operate or store the LCD module under outside of specified environmental conditions.
(2) As electrical impedance of power supply lines (VCC-VSS) are low when LCD module is working, place the de-coupling capacitor near by LCD module as close as possible.
(3) Reset signal must be sent after power on to initialize LSI. LSI does not function properly until initialize it by reset signal.
(4) Generally, at power on, in order not to apply DC charge directly to LCD panel, supply logic voltage first and initialize LSI logic function including polarity alternation. Then supply voltage for LCD bias. At power off, in order not to apply DC charge directly to LCD panel, execute Power OFF sequence and Discharge command.
(5) Don't touch to FPC surface, exposed IC chip, electric parts and other parts, to any electric, metallic materials.

(6) No bromide specific fire-retardant material is used in this module.
(7) Do not display still picture on the display over 2 hours as this will damage the liquid crystal.
(8) Be sure to use a power supply with the safety protection circuit such as the fuse for excess voltage, excess current, electric discharge waveform and Latch-up occurring.
(9) Epoxy resin (amine series curing agent), silicone adhesive material (dealcoholization series and oxime series), tray forming agent (azo compound) etc, in the cabinet or the packing materials may induce abnormal display with polarizer film deterioration regardress of contact or noncontact to polarizer film.
Be sure to confirm the component of them.

[Precautions for Discarding Liquid Crystal Modules]

COG: After removing the LSI from the liquid crystal panel, dispose of it in a similar way to circuit boards from electronic devices.
LCD panel: Dispose of as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances. The liquid crystal panel only contains an extremely small amount of liquid crystal (approx.100mg) and therefore it will not leak even if the panel should break.
-Its median lethal dose (LD50) is greater than 2,000 mg/kg and a mutagenic (Aims test: negative) material is employed.
FPC: Dispose of as similar way to circuit board from electric device.

1. Application

This data sheet is to introduce the specification of LS055T3SX05 active matrix 16,777,216color LCD module.
Main color LCD module is controlled by Driver IC (RSP R63417).
If any problem occurs concerning the items not stated in this temporary specification, it must be solved sincerely by both parties after deliberation.
As to basic specification of driver IC refer to the IC specification and handbook.

2. Construction and Outline

Construction: LCD panel, Driver (COG), FPC with electric components, 12 White LED lump, prism sheet, diffuser, light guide and reflector, plastic frame to fix them mechanically.
Outline: See page 32
Connection: B to B connector ;LCD side:Panasonic AXE640124,user side:Panasonic AXE540124

There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function.

In order to realize thin module structure, double-sided adhesive tapes are used to fix LCD panels. As these tapes do not guarantee to permanently fix the panels, LCD panel may rise from the module when shipped from factory.
So please make sure to design the system to hold the edges of LCD panel by the soft material such as sponge when LCD module is assembled into the cabinet.

3. Mechanical Specification

Table 1

Parameter		Specifications	Unit
Outline dimension(typ)		70.44(W)×129.59 (H)×1.46(D)	mm
Main LCD Panel	Display mode	New Mode2	
	LCD mode	Transmissive	
	Active area	68.04(W)×120.96(H)	mm
	Display format	1080×RGB(W)×1920(H)	-
	Dot pitch	0.021(W)×0.063 (H)	mm
	Base color Note1	Normally Black	-
Mass		About 27	g

*1 Due to the characteristics of the LC material, the colors vary with environmental temperature.

4. Absolute Maximum Ratings

(4-1) Electrical absolute maximum ratings

Table 2

Item	Symbol	Rating	Unit	Remark
Power Supply voltage(1)	IOVDD-GND	-0.3 to +3.3	V	Note 1,2
Power Supply voltage(2)	AVDD+ -AGND	-0.3 to +6.0	V	Note 1,2
Power Supply voltage(3)	AGND- AVDD-	-0.3 to +6.0	V	Note 1,2

Note:

1. Connect these power supplies to other power supplies on the FPC when they are set at the same electrical potential as other power supplies. For voltage, see DC Characteristics in Electrical Characteristics.
2. The voltage of this terminal should not exceed DPHYVCC.

(4-2) Environment Conditions

Table 3

Item	Top		Tstg		Remark
	Min	Max	Min	Max	
Ambient temperature	-20°C	+60°C	-30°C	+70°C	Note2
Humidity	Note1		Note1		No condensation

Note :

1. Ta ≤ 40 °C.....90 % RH Max
2. Ta > 40 °C.....Absolute humidity shall be less than Ta=40 °C /90 % RH.

As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable. Be sure not to exceed the rated voltage, otherwise a malfunction may occur.

5. Electrical Specifications

(5-1) Power Supply Voltage Range

Table 4

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply voltage	AVDD+	4.85	5.0	5.15	V	note 1
Supply voltage	AVDD-	-5.15	-5.0	-4.85	V	note 1
Supply voltage	IOVDD	1.65	1.8	1.95	V	note 1

Notes: 1. The DC/AC electrical characteristics of bare die and wafer are guaranteed at +60·C.

(5-2) DC characteristics

Table 5

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Remark
Input high-level voltage 1		V_{IH1}	IOVDD=1.650V ~ 1.950V	0.70x IOVDD	-	IOVDD	V	note 1,2
Input low-level voltage 1		V_{IL1}	IOVDD=1.650V ~ 1.950V	0	-	0.30x IOVDD	V	
Output high-level voltage 1(LEDPWM)		V_{OH1}	IOVDD=1.650V ~ 1.950V, IOUT = -0.1mA	0.80x IOVDD	-	-	V	note 1
Output high-level voltage 1(LEDPWM)		V_{OL1}	IOVDD=1.650V ~ 1.950V, IOUT = 0.1mA	-	-	0.20x IOVDD	V	
Input high-level current		I_{IH}	Vin=IOVDD	-	-	10	uA	
Input low-level current		I_{IL}	Vin=0V	-10	-	-	uA	
Current consumption	Normal Mode	I_{IOVDD}	All pixels white	-	10.3	15.5	mA	note 2 note 3
		I_{AVDD+}		-	7.8	11.7	mA	
		I_{AVDD-}		-	5.6	8.4	mA	
	Deep Standby Mode	I_{IOVDD}	N/A	-	0.01	0.02	mA	
		I_{AVDD+}		-	0.01	0.02	mA	
		I_{AVDD-}		-	0.01	0.02	mA	

Note:

1. The DC/AC electrical characteristics of Module are guaranteed at -20° C ~ +60° C.
2. Conditions: Ta=25℃,AVDD+ =5.0V,AVDD- =-5.0V,IOVDD=1.8V,MIPI-DSI CMD Mode(still picture),Refresh rate=58Hz
3. Conditions :CLK+/-,Data0+/-, Data1+/-, Data2+/-, Data3+/- :LP 11 Mode

(5-3) MIPI DSI characteristics

Table 6

Item		Symbol	Unit	Test Condition	Min.	Typ.	Max.	Notes
HS-RX	Differential input high threshold	VIDTH	mV	IOVDD=DPHYVCC =1.65V ~ 1.95V	-	-	70	3
	Differential input low threshold	VIDTL	mV	IOVDD=DPHYVCC =1.65V ~ 1.95V	-70	-	-	3
	Single-ended input low voltage	VILHS	mV	IOVDD=DPHYVCC =1.65V ~ 1.95V	-40	-	-	
	Single-ended input high voltage	VIHHS	mV	IOVDD=DPHYVCC =1.65V ~ 1.95V	-	-	460	
	Common-mode voltage HS receive mode	VCMRX(DC)	mV	IOVDD=DPHYVCC =1.65V ~ 1.95V	70	-	330	1
	Differential input impedance	ZID	Ω	IOVDD=DPHYVCC =1.65V ~ 1.95V	-	100	-	2
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV	IOVDD=DPHYVCC =1.65V ~ 1.95V	-50	-	550	
	Logic 1 input voltage	VIH	mV	IOVDD=DPHYVCC =1.65V ~ 1.95V	880	-	1350	
	I/O leakage current	ILEAK	uA	Vin= -50mV-1350mV	-10	-	10	
LP-TX	Thevenin output low level	VOL	mV	IOVDD=DPHYVCC =1.65V ~ 1.95V	-50	-	50	
	Thevenin output high level	VOH	V	IOVDD=DPHYVCC =1.65V ~ 1.95V	1.1	1.2	1.3	
	Output impedance of LP transmitter	ZOLP	Ω	IOVDD=DPHYVCC =1.80V	110	-	-	2
CD-RX	Logic 0 contention threshold	VILCD	mV	IOVDD=DPHYVCC =1.65V ~ 1.95V	-	-	200	
	Logic 1 contention threshold	VIHCD	mV	IOVDD=DPHYVCC =1.65V ~ 1.95V	450	-	-	

Note:

1. VCMRX (DC) = (VP+VDN)/2.
2. Excluding COG resistance (contact resistance and ITO wiring resistance). The values are tentative
3. Minimum 110mV/-110mV HS differential swing is required for display data transfer

Table 7: MIPI DSI HS-RX Clock and Data-Clock Specifications

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Notes
DSICLK Frequency	fDSICLK	MHz	IOVDD=DPHYVCC= 1.65V ~ 1.95V	100	-	500	1
DSICLK Cycle time	tCLKP	ns	IOVDD=DPHYVCC= 1.65V ~ 1.95V	1	-	10	
DSI Data Transfer Rate	tDSIR	Mbps	IOVDD=DPHYVCC= 1.65V ~ 1.95V DSI 2 lanes,3 lanes, 4lane	200	-	1000	1
Data to Clock Setup Time	tSETUP	UI	IOVDD=DPHYVCC= 1.65V ~ 1.95V	0.15	-	-	3
		ns	IOVDD=DPHYVCC= 1.65V ~ 1.95V	0.15	-	-	2,3
Clock to Data Hold Time	tHOLD	UI	IOVDD=DPHYVCC= 1.65V ~ 1.95V	0.15	-	-	3
		ns	IOVDD=DPHYVCC= 1.65V ~ 1.95V	0.15	-		2,3

Note:

1. When fDSICLK<125MHz, change auto load NV setting so that it is compliant with THS-PREPARE+THS-ZERO spec.
2. Minimum tSETUP/tHOLD Time is 0.15UI. This value may change according to DSI transfer rate.
3. tSETUP/tHOLD Time are measured without HS-TX Jitter.

Table 8: MIPI DSI LP-RX/TX Clock and Data-Clock Specifications

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Notes
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$		IOVDD=DPHYVCC= 1.65V ~ 1.95V	40ns + 4*UI	-	85ns + 6*UI	
$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	$T_{HS-PREPARE}$ + $T_{HS-ZERO}$		IOVDD=DPHYVCC= 1.65V ~ 1.95V	145ns +10*UI	-	-	
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$		IOVDD=DPHYVCC= 1.65V ~ 1.95V	max (n*8*UI, 60ns + n*4*UI)	-	-	1,2
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	ns	IOVDD=DPHYVCC= 1.65V ~ 1.95V	100	-	-	
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		IOVDD=DPHYVCC= 1.65V ~ 1.95V	4*T LPTX			
Time-out before new TX side starts driving	$T_{TA-SURE}$		IOVDD=DPHYVCC= 1.65V ~ 1.95V	1*T_{LPTX}		2* T_{LPTX}	
Time to drive LP-00 by new TX	T_{TA-GET}		IOVDD=DPHYVCC= 1.65V ~ 1.95V	5* T_{LPTX}			
Length of any Low-Power state period	T_{LPX}	ns	IOVDD=DPHYVCC= 1.65V ~ 1.95V	50	-	-	
Ratio of $T_{LPX(MASTER)}$ /$T_{LPX(SLAVE)}$ between Master and Slave side	Ratio T_{LPX}		IOVDD=DPHYVCC= 1.65V ~ 1.95V	2/3	-	3/2	
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$		IOVDD=DPHYVCC= 1.65V ~ 1.95V	60ns + 52*UI	-	-	3
$T_{CLK-PREPARE}$ +time for lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	ns	IOVDD=DPHYVCC= 1.65V ~ 1.95V	300	-	-	
Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	UI	IOVDD=DPHYVCC= 1.65V ~ 1.95V	8	-	-	
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	ns	IOVDD=DPHYVCC= 1.65V ~ 1.95V	38	-	95	
Time to drive HS differential state after last payload clock bit of an HS transmission burst	$T_{CLK-TRAIL}$	ns	IOVDD=DPHYVCC= 1.65V ~ 1.95V	60	-	-	
Time from start of THS-TRAIL period to start of LP-11 state	T_{EOT}		IOVDD=DPHYVCC= 1.65V ~ 1.95V	-	-	105ns + n*12*UI	2
Length of Low-Power TX period in case of using DSI clock	T_{LPTX1}	UI	IOVDD=DPHYVCC= 1.65V ~ 1.95V	-	32	-	4
Length of Low-Power TX period in case of using internal OSC clock	T_{LPTX2}	ns	IOVDD=DPHYVCC= 1.65V ~ 1.95V	-	1/(fosc /2)	-	

Note:

1. If a > b then max(a, b) = a, otherwise max(a, b) = b.
2. Where n = 1 for Forward-direction HS mode.
3. The R63417 can work with this specification although the end part of internal process is remained when Clock Lane enter LP-11 and the R63417 can work without the remained process if tCLK-POST is more than 256 UI.
4. The R63417 uses DSI clock from the Host processor if Clock Lane is active, and internal oscillator clock if Clock Lane is disabled. Here, "fosc" is the frequency of oscillator clock, typical 56 MHz.

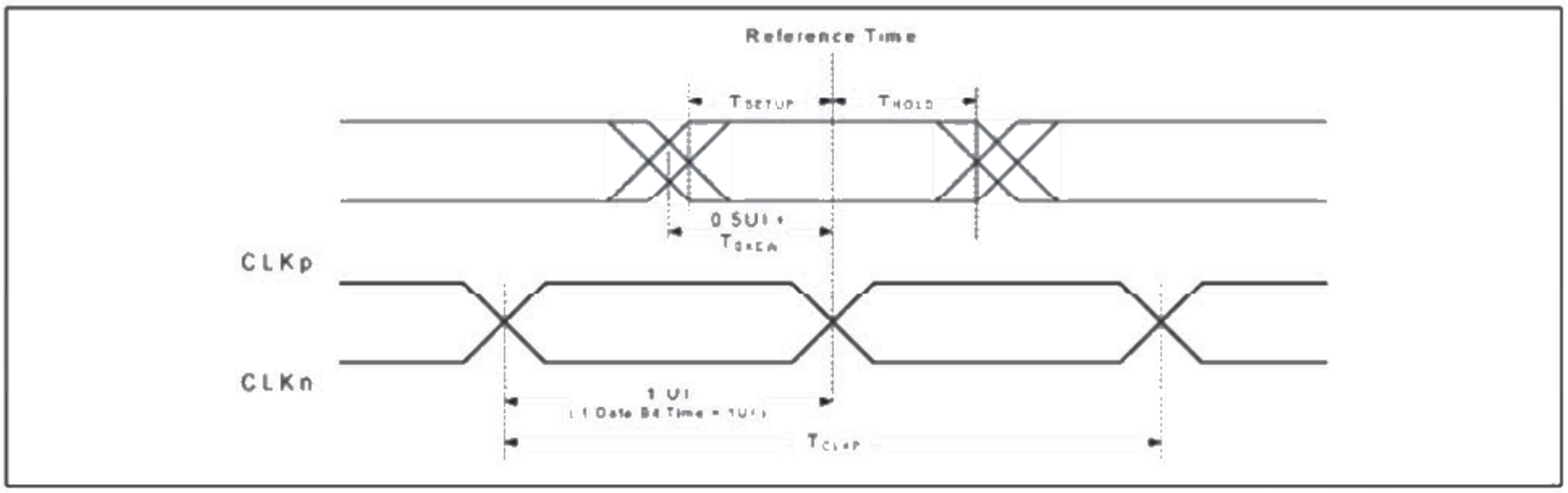


Fig.1 Data to Clock Timing Definitions

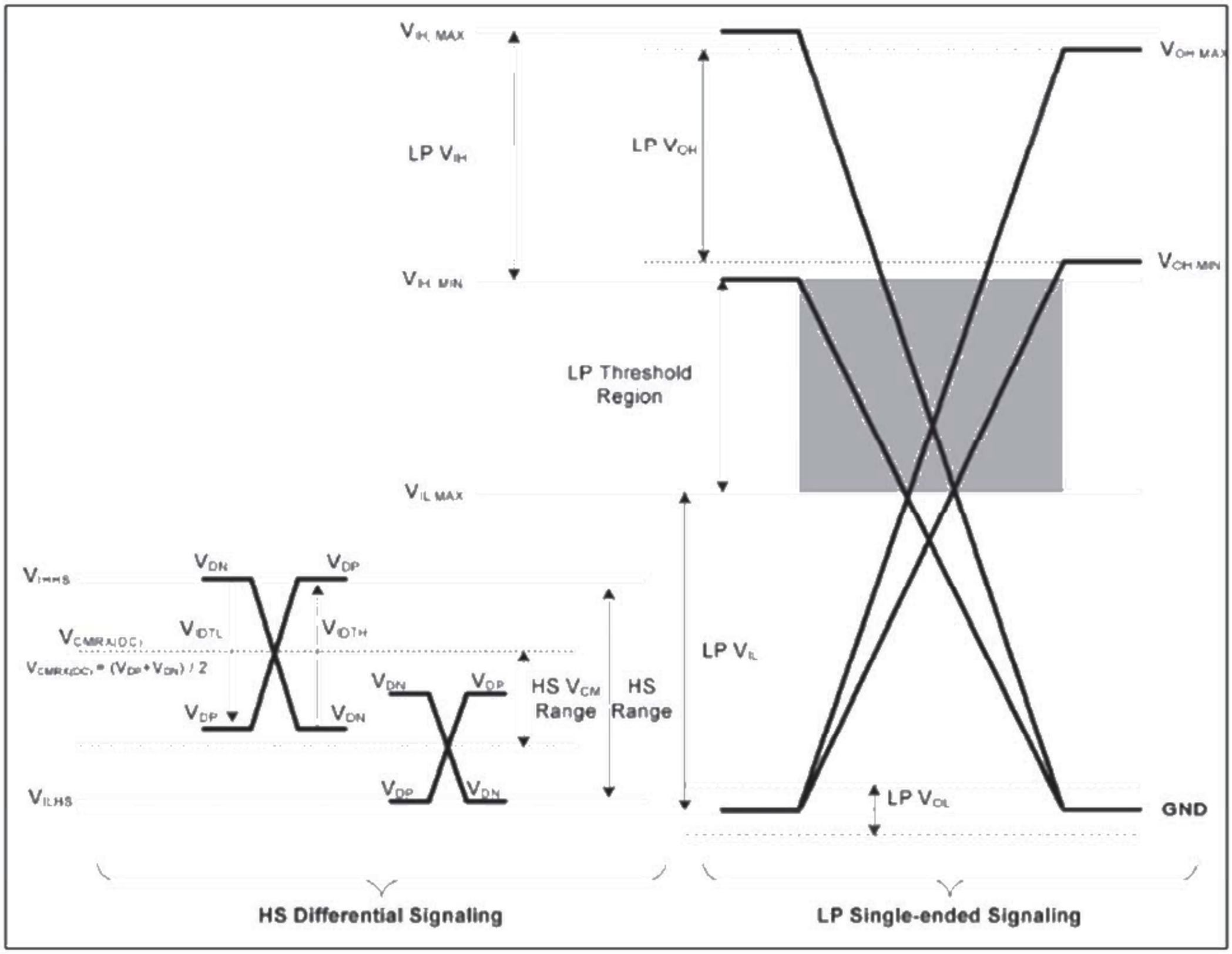


Fig.2 DSI LP Mode

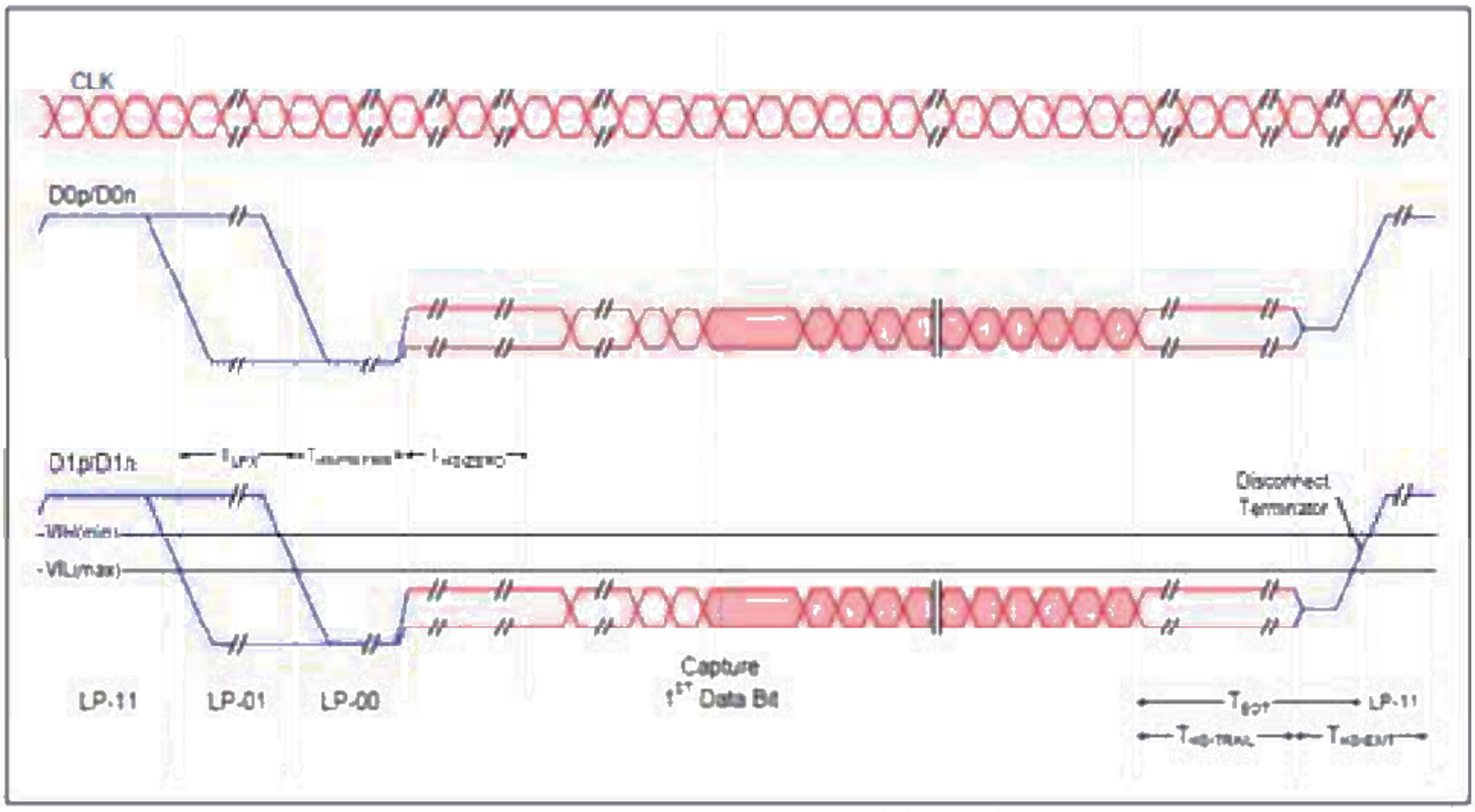


Fig.3 HS Data Transmission in Bursts

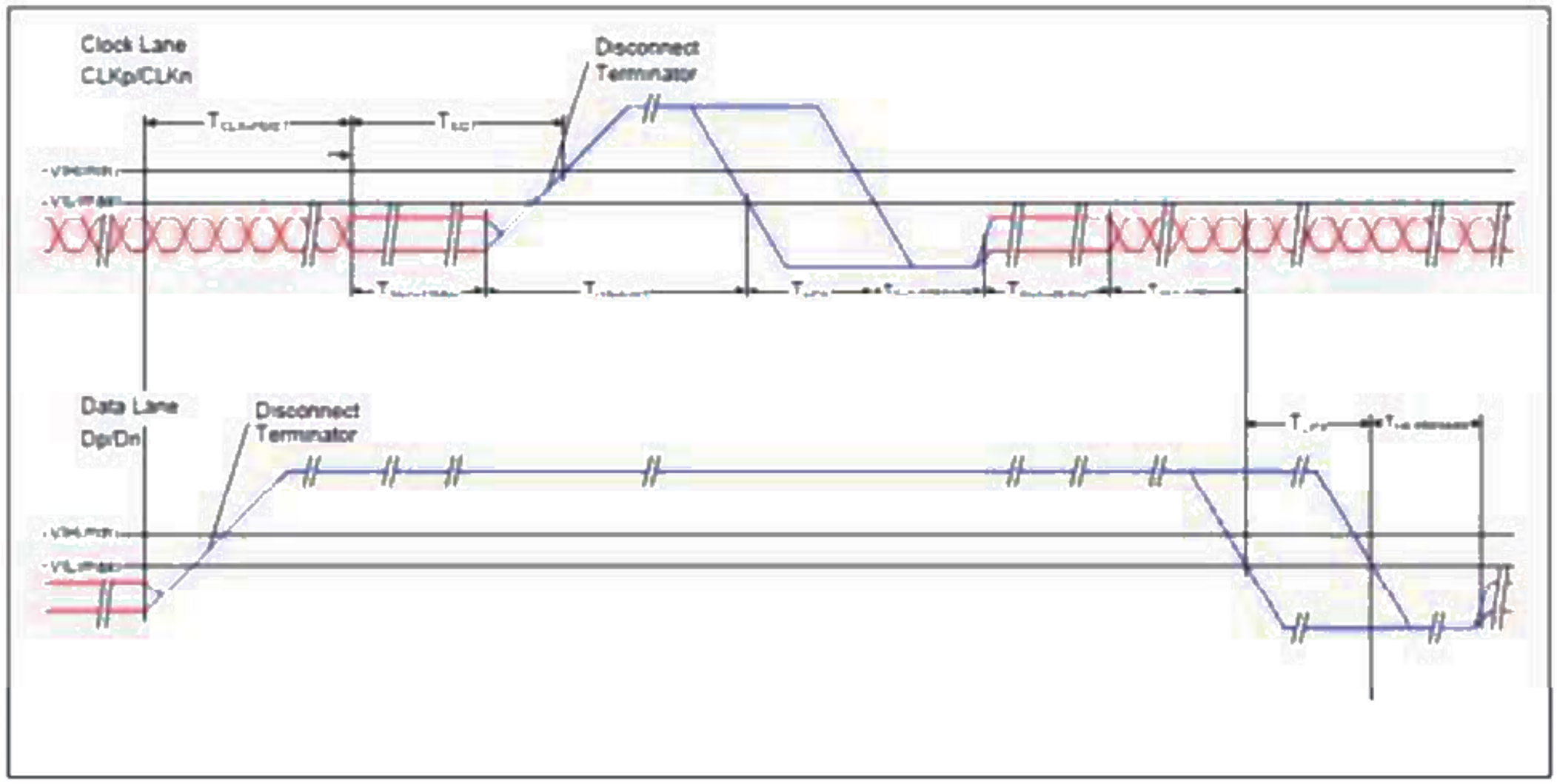
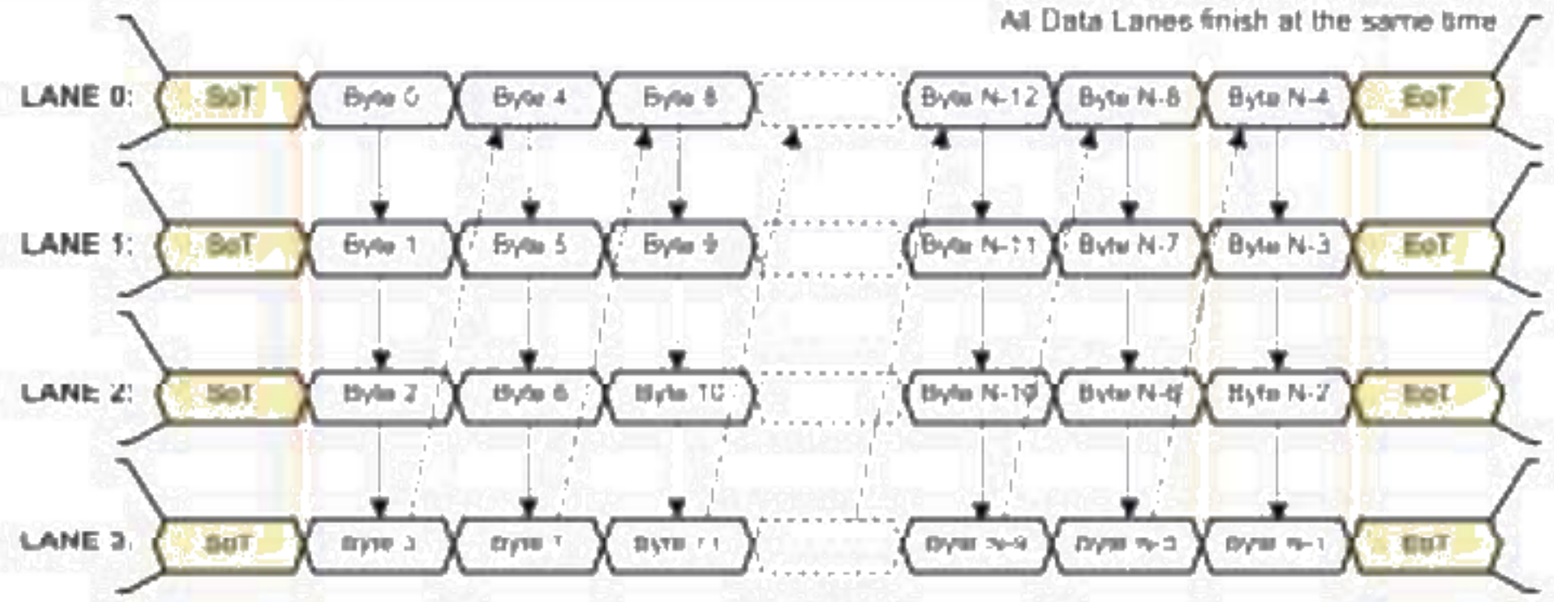
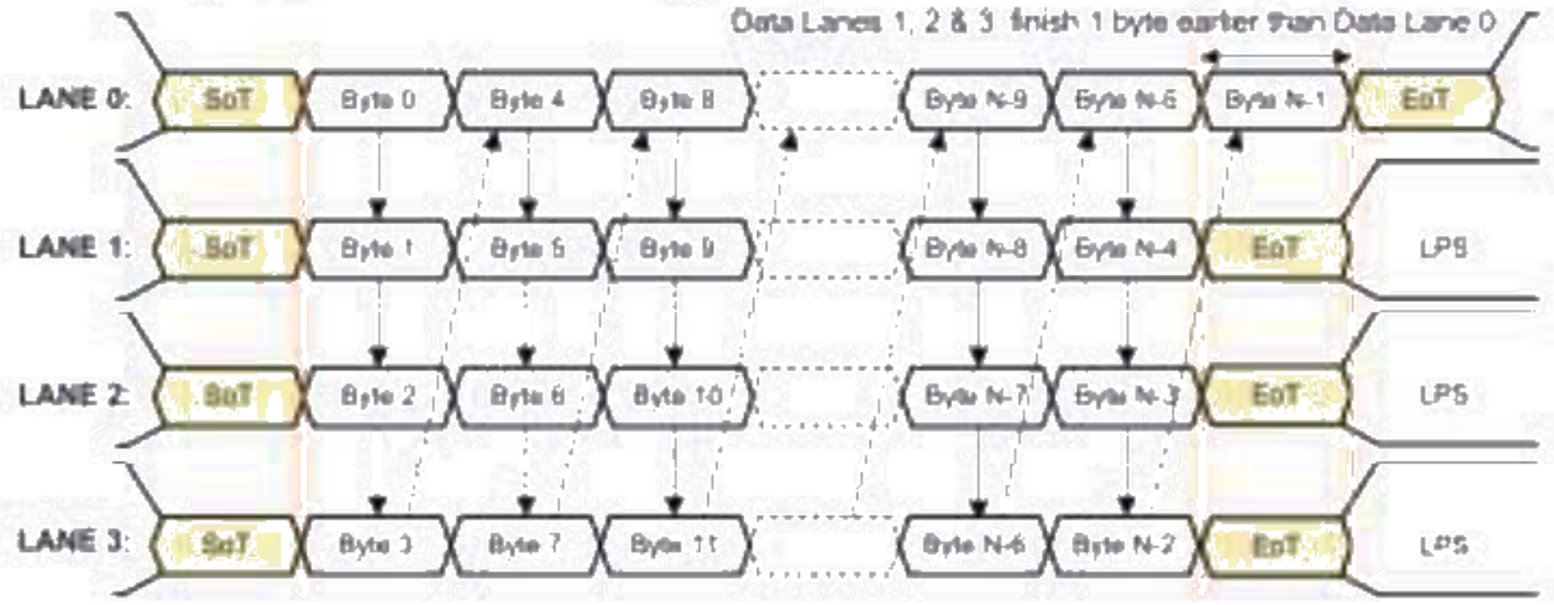


Fig.4 Switching the Clock Lane between Clock Transmission and LP Mode

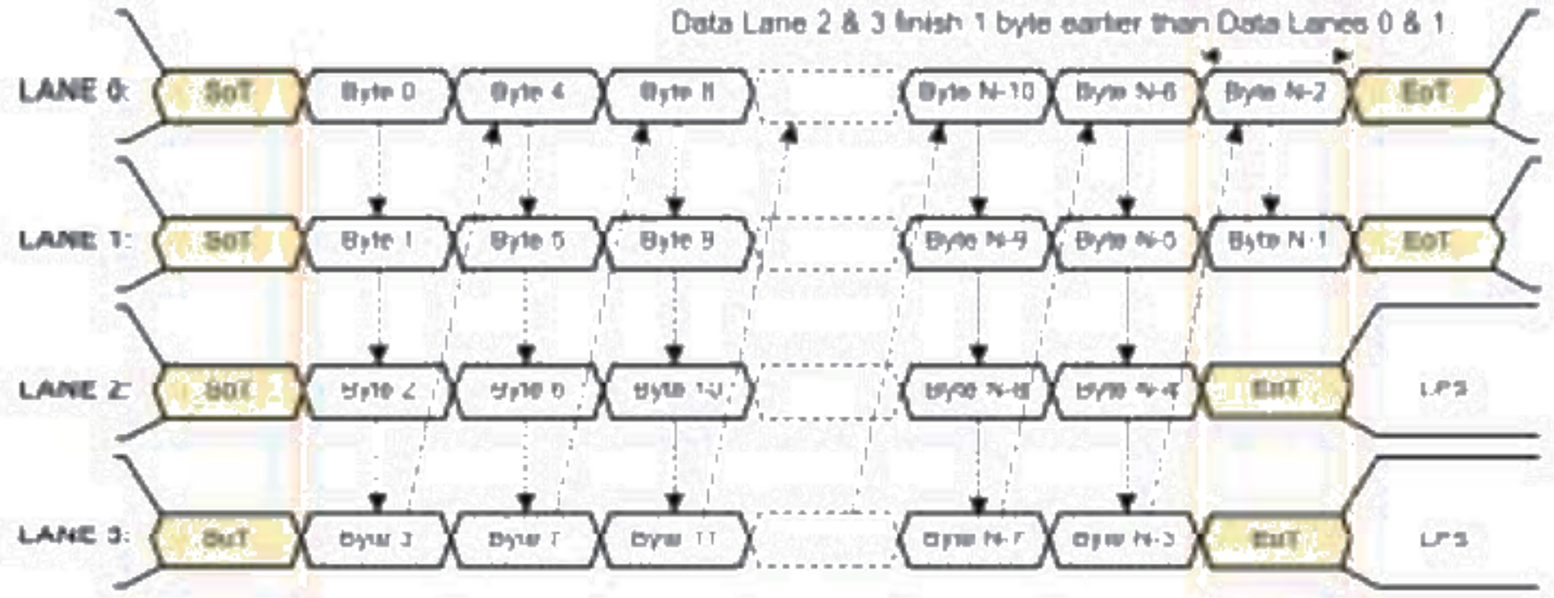
Number of Bytes, N, transmitted is an integer multiple of the number of lanes:



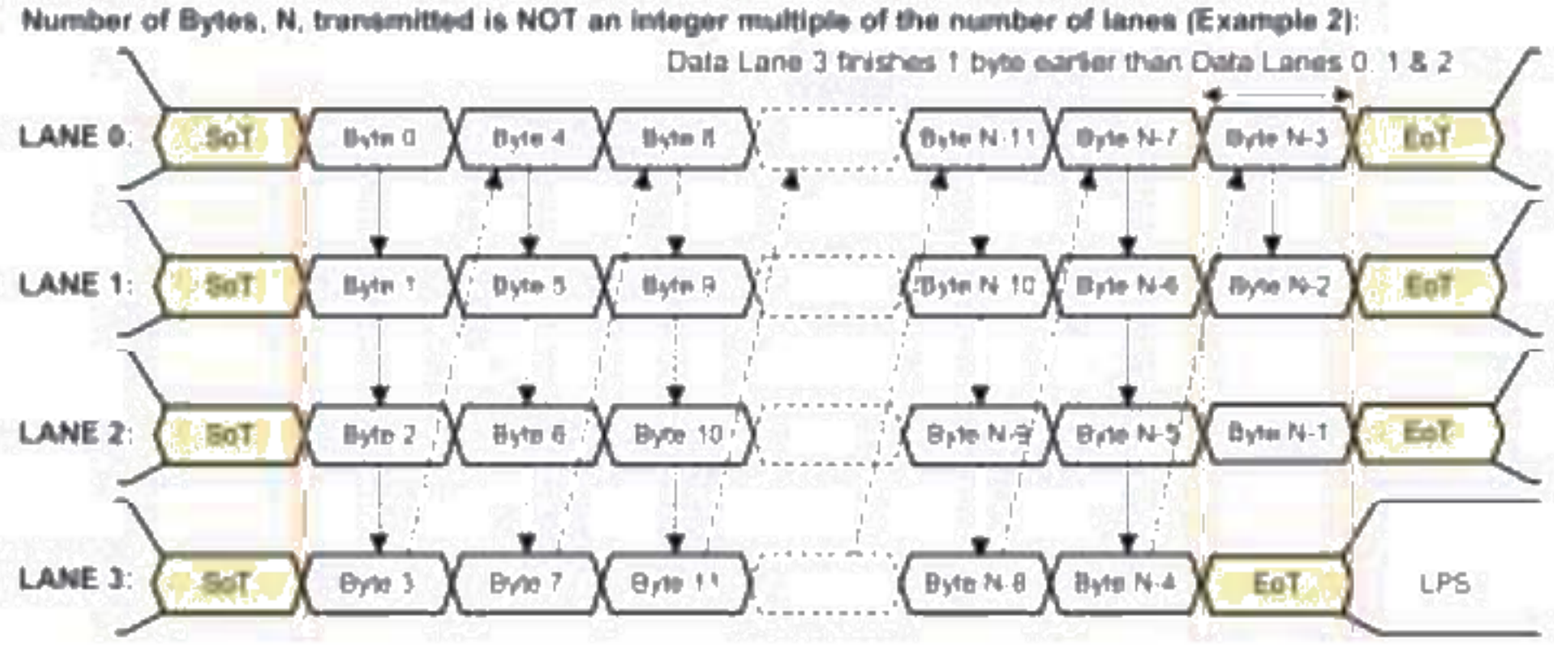
Number of Bytes, N, transmitted is NOT an integer multiple of the number of lanes (Example 1):



Number of Bytes, N, transmitted is NOT an integer multiple of the number of lanes (Example 2):



Number of Bytes, N, transmitted is NOT an integer multiple of the number of lanes (Example 2):



KEY:
LPS – Low Power State SoT – Start of Transmission EoT – End of Transmission

Fig.5 Four Lanes HS Transmission Example

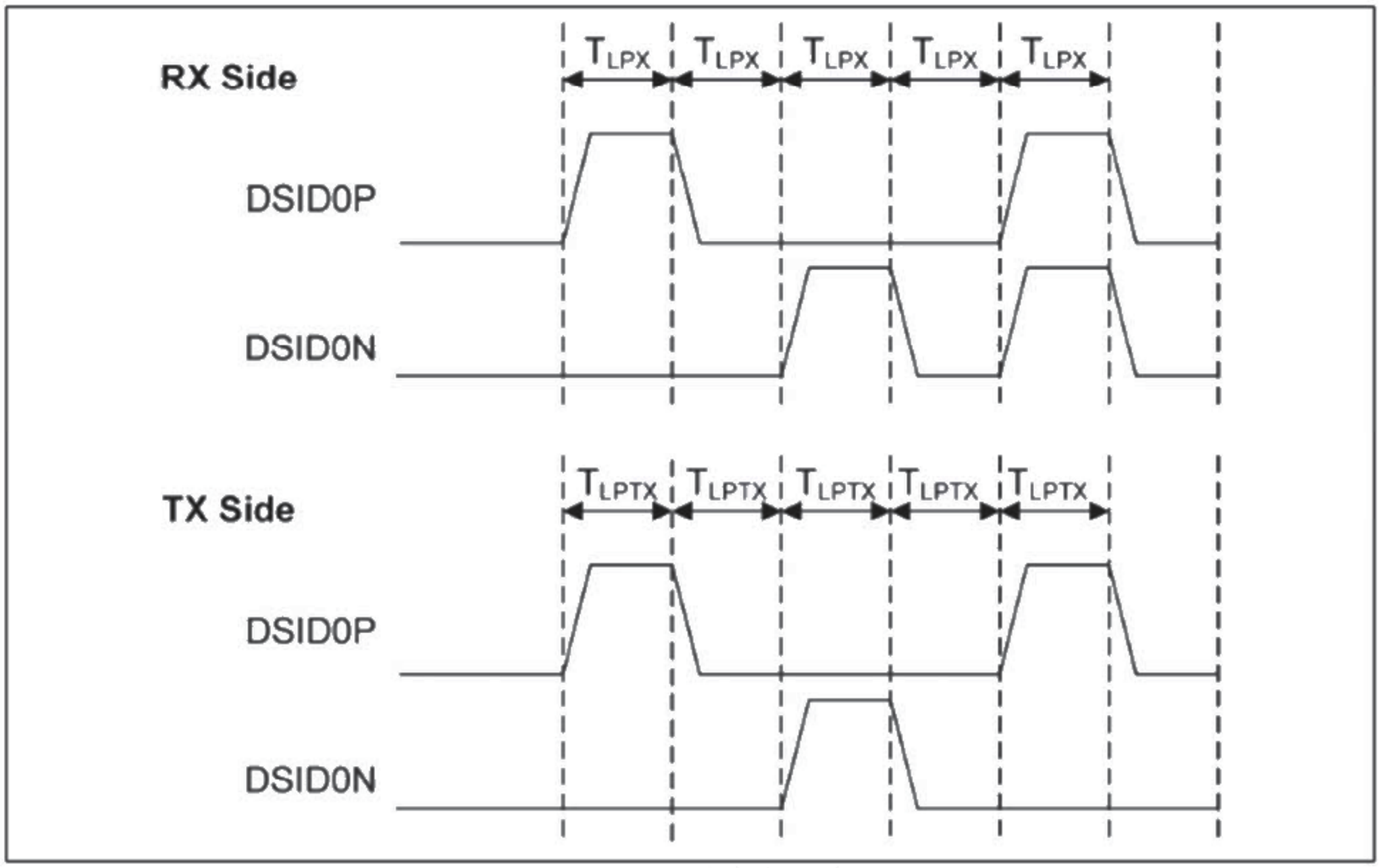


Fig.6 DSI LP Mode

(5-4) LED backlight

At main panel the back light uses 12pcs edge light type white LED.

Table 9

Item	Value(1 parallel)			Unit
	Min	Nominal	Max	
Forward current	-	20	30	mA
Number of LED components	12pcs LED(6pcs*2parallel)			

LED made by SHARP

*Please consider Allowable Forward Current on used temperature

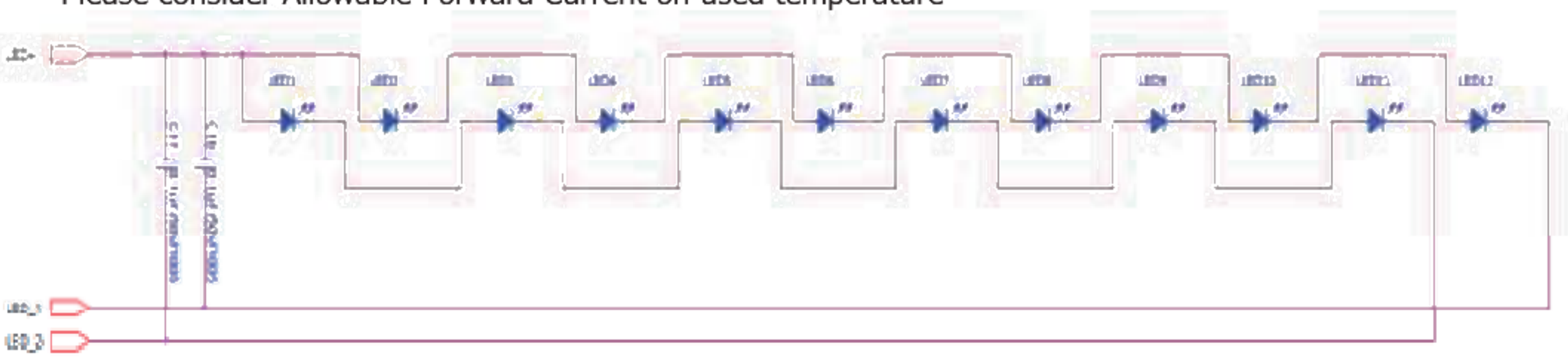


Fig.7 Schematics drawing of lighting

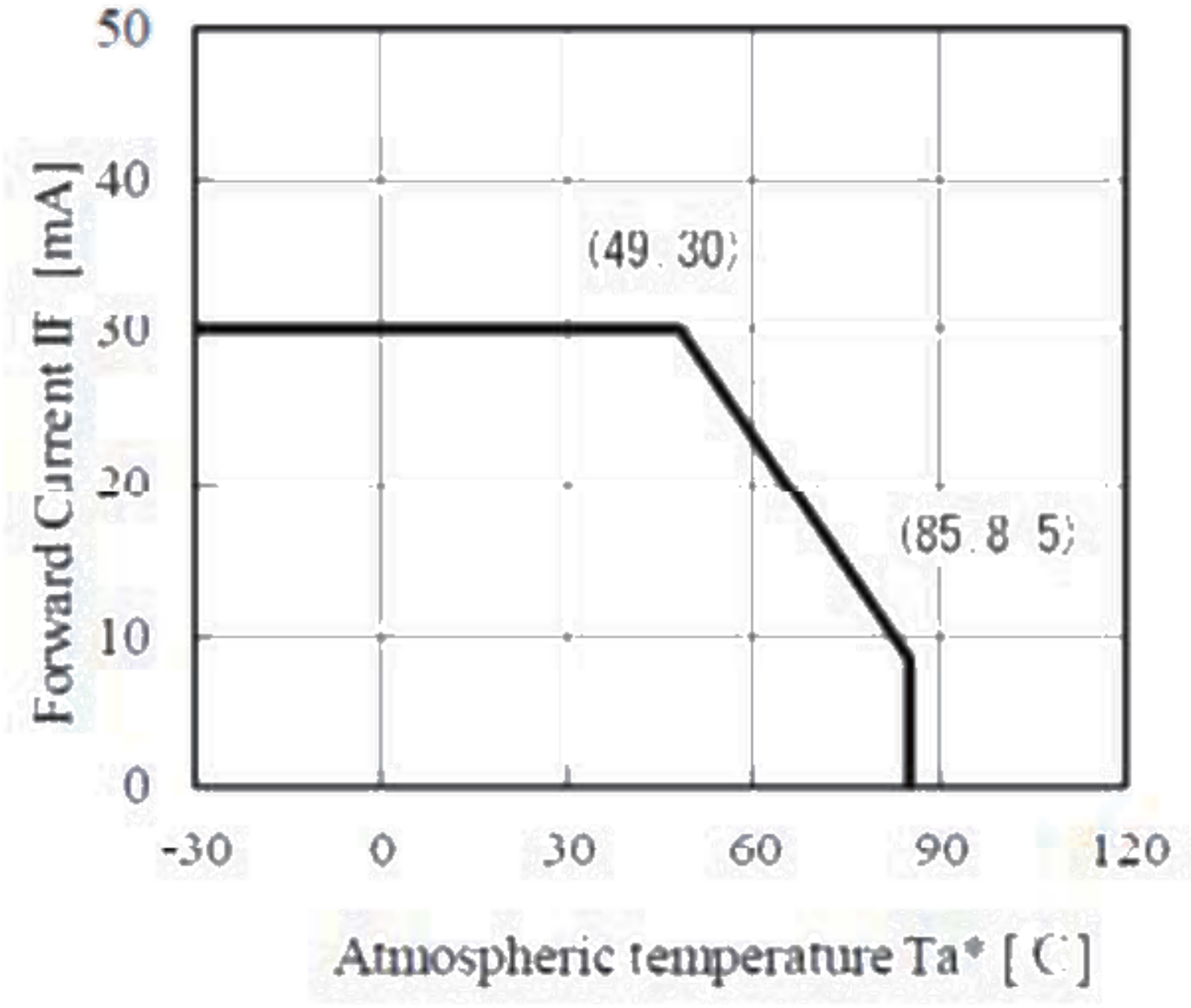


Fig.8 Forword Current Derating Curve

(5-5) Interface signals

Table 10

Pin No	Symbol	Description	I/O	Remarks
1	GND	GND level pin	-	
2	DATA_3N	MIPI data3 signal line (-)	I	
3	DATA_3P	MIPI data3 signal line (+)	I	
4	GND	GND level pin	-	
5	DATA_0N	MIPI data0 signal line (-)	I/O	
6	DATA_0P	MIPI data0 signal line (+)	I/O	
7	GND	GND level pin	-	
7	CLK_N	MIPI clock signal line (-)	I	
9	CLK_P	MIPI clock signal line (+)	I	
10	GND	GND level pin	-	
11	DATA_1N	MIPI data1 signal line (-)	I	
12	DATA_1P	MIPI data1 signal line (+)	I	
13	GND	GND level pin	-	
14	DATA_2N	MIPI data2 signal line (-)	I	
15	DATA_2P	MIPI data2 signal line (+)	I	
16	GND	GND level pin	-	
17	ID0 (GND)	ID code	-	ID0=″0″
18	ID1 (GND)	ID code	-	ID1=″0″
19	XRES	Reset pin	I	″L″ Active
20	TE	Tearing effect output signal pin	O	
21	IOVDD	Power supply for LCD(IO,Logic)	I	IOVDD = 1.8±0.15V
22	AVDD+	Power supply for LCD(Source driver and VCOM)	I	AVDD+ = 5.0±0.15V
23	GND	GND level pin	-	
24	AVDD-	Power supply for LCD(Source driver and VCOM)	I	AVDD- = -5.0V±0.15V
25	HSYNC	Horizontal signal to synchronize LCD drive	O	
26	LED_PWM	Backlight LED driver PWM	O	
27	GND	GND level pin	-	
28	GND	GND level pin	-	
29	LED+	Power supply for LED (Anode)	I	
30	LED+	Power supply for LED (Anode)	I	
31	LED_1-	Power supply for LED (Cathode)	I	
32	LED_2-	Power supply for LED (Cathode)	I	
33	GND	GND level pin	-	
34	NC	Open pin	-	
35	NC	Open pin	-	
36	NC	Open pin	-	
37	NC	Open pin	-	
38	NC	Open pin	-	
39	NC	Open pin	-	
40	GND	GND level pin	-	

Notes:
The direction is named with respect to the display module, I = from host to module, O = from module to host.

Table 11: Connector description

Assembled on	Item	Description
Phone PWB	Connector type	BtoB
	Pin amount	40
	Manufacturer	panasonic
	Part number	AXE540124

(5-6) Reset Timing Characteristics

Table 12

Item	Symbol	Unit	Test condition	Min.	Max.
Reset low-level width1	tRW1	us	Power supply on	1000	–
Reset low-level width2	tRW2	us	Operation	1000	–
Reset time (Sleep IN)	tRT1	ms	–	–	3
Reset time (Sleep OUT)	tRT2	ms	–	–	3
Noise reject width	tRESNR	us	–	–	1

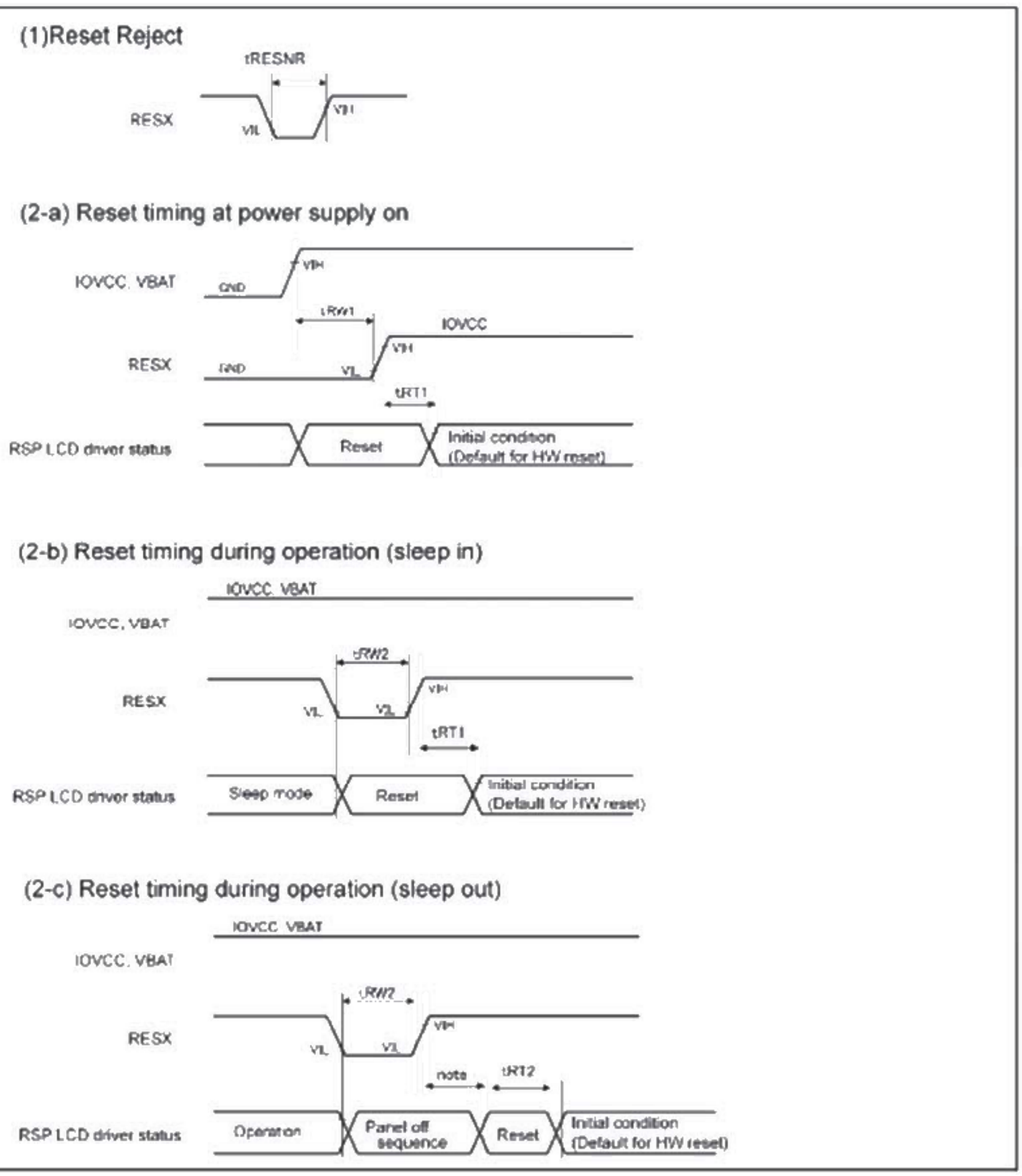


Fig.9 Reset Timing Characteristics

(5-7) Schematic of LCD module system

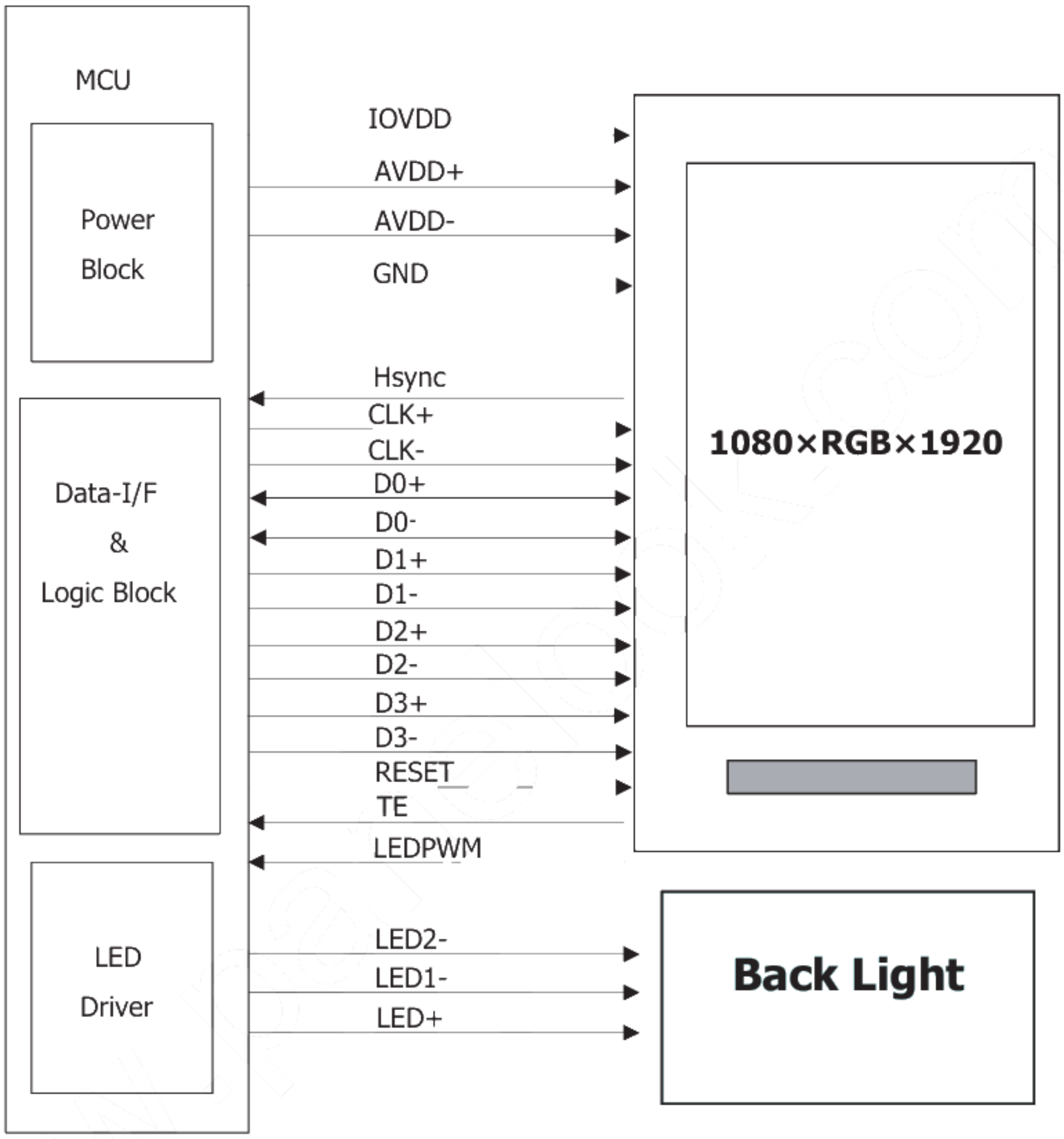


Fig.10 Schematic of LCD module system

6. Initial Sequence

Table 13: Condition

I/F:MIPI DSI 4lane,Command/Video Mode
Dots Size:1080xRGBx1920
Power Supply: IOVDD=1.8V,AVDD+ =5.0V,AVDD- =-5.0V
Color Mode:24 bit
Frame frequency: TYP 58HZ

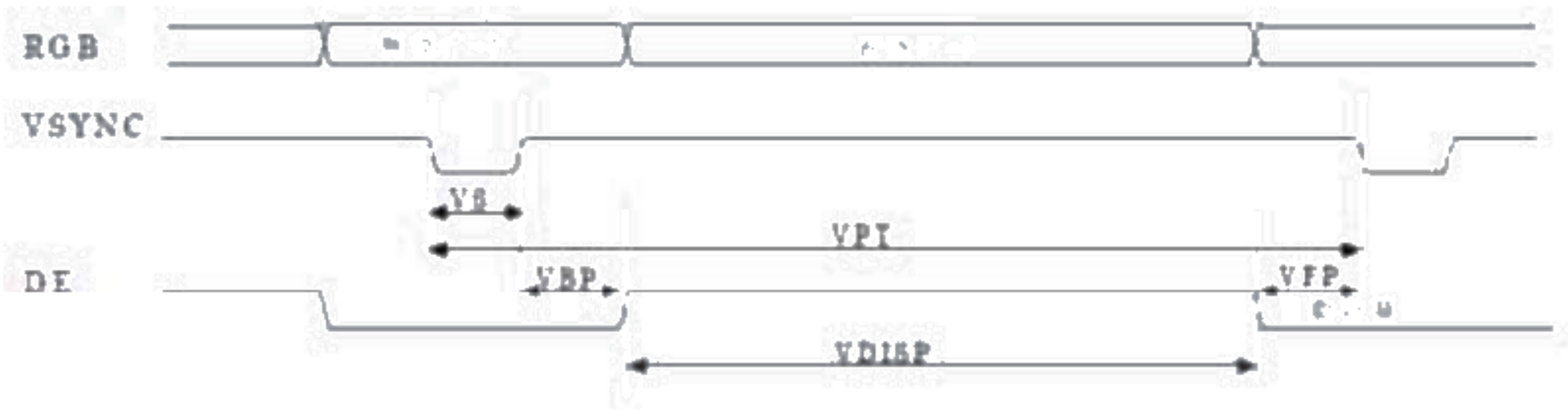


Fig.11 Schematic Diagram of Video Timing

Table 14: Video Timing

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Verticle cycle	VPT	VDISP+VBLK		1930	-	Line
Verticle low pulse width	VS		-	2	-	Line
Vertical front porch	VFP		-	4	-	Line
Vertical back porch	VBP		-	4	-	Line
Vertical data start point		VS+VBP	-	6	-	Line
Vertical blanking period	VBLK	VS+VBP+VFP	-	10	-	Line
Vertical active area		VDISP	-	1920	-	Line
Vertical Refresh Rate	VRR		55.00	58.00	61.00	Hz

Ta=-20℃~+60℃, IOVDD=1.8V, AVDD+=5.0V, AVDD-=-5.0V, GND=0V

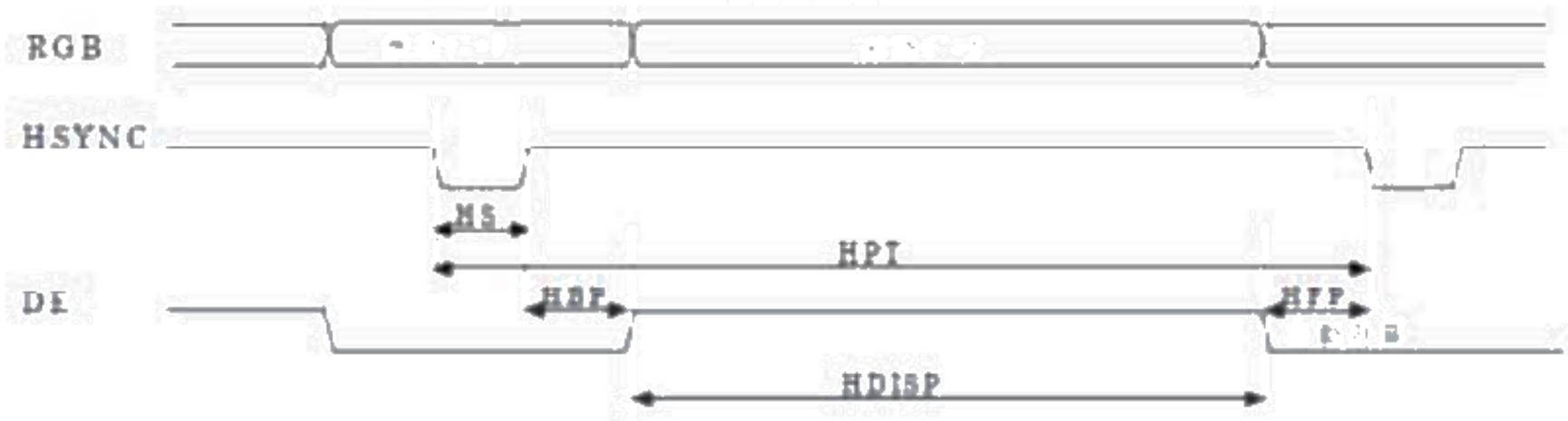


Fig.12 Schematic Diagram of Video Timing

Table 15: Video Timing

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
HS cycle	HPT	HDISP+HBLK	-	1282	-	PCLK
HS low Pulse width	HS		-	10	-	PCLK
Horizontal back porch	HBP		-	50	-	PCLK
Horizontal front porch	HFP		-	142	-	PCLK
Horizontal data start point		HS+HBP	-	60	-	PCLK
Horizontal blanking period	HBLK	HS+HBP+HFP	-	202	-	PCLK
Horizontal active area	HDISP		-	1080	-	PCLK
1 Horizontal Timing			-	8.928	-	us
Pixel clock frequency	PCLK		136	143.60	151	MHz
MIPI Speed	-	-	950	1000	1050	Mbps/lane

Ta=-20℃~+60℃, VDDI=1.8V, AVDD+=5.0V, AVDD-=-5.0V, GND=0V

Table 14: Power ON Sequence(power on→Normal)

ITEM	Modified Driver IC		REMARK
	Register Address	Register Data list	
RESX (RESX ="L")			
IOVDD=1.8V			
WAIT 10ms (min 5ms)			
AVDD+ =5.0V			
WAIT 10ms (min 0ms)			
AVDD-=-5.0V			
WAIT 10ms (min 3ms)			
RESX (RESX ="H")			
Wait 10ms (min 3ms)			
NVM Protect OFF			
Manufacturer Command Access Protect	B0h	04h	
Interface Setting	B3h	**h	04h Command mode 35h Video mode
		00h	Interface setting
		00h	
		22h	
		00h	
		00h	
NVM LOAD	D6h	01h	
Set_pixel_format	3Ah	77h	24 bits/pixel (16,777,216 colors)
Column Address	2Ah	00h 00h 04h 37h	(Only command mode)
Page Address	2Bh	00h 00h 07h 7Fh	(Only command mode)
Set_tear_on	35h	00h	Vsync On (Only command mode)
Display pattern	2C/3C	**	Black pattern (Only command mode)
SLEEP OUT			
SLPOUT	11h	-	
DSI Vedio mode transfer start			
WAIT MIN 120ms			[Automatic] Sleep Mode Off
Display On			
DISPON	29h	-	

BackLight ON			
Write_display_brightness	51h	0x00	0FFh:LED light=100%
		0XFF	
Write_content_adaptive_brightness_control	55h	0x**	CABC OFF=00h CABC ON=02h
Write_control_display (BackLight On)	53h	0x2C	LED(PWM) On
Display pattern			

Table 15: Power OFF Sequence(Normal→power off)

ITEM	Register Address	Register Data list	REMARK
BackLight OFF			
Write_control_display (BackLight Off)	53h	0x00	LED(PWM) Off
Display Off			
DISPOFF	28h	-	
WAIT MIN 20ms			
SLEEP IN			
SLPIN	10h	-	
WAIT MIN 120ms			
DSI Vedio mode transfer stop			
RSX (RESX ='L')			
WAIT 10ms (min 3ms)			
AVDD- OFF			
WAIT 10ms (min 0ms)			
AVDD+ OFF			
WAIT 10ms (min 5ms)			
IOVDD OFF			

Table 16: Deep standby In sequence (Normal→Deep standby In sequence)

ITEM	Register Address	Register Data list	REMARK
BackLight OFF	0x53	0x00	
Display OFF	0x28	-	
WAIT 20ms(min)			
Sleep IN	0x10	-	
WAIT 120ms(min)			
Manufacturer Command Access Protect	0xB0	0x02	
Deep standby in	0xB1	0x01	
DSI Video mode transfer stop			
WAIT 10ms (min 3ms)			
AVDD- OFF			
WAIT 10ms (min 0ms)			
AVDD+ OFF			

Table 17: Deep standby out sequence (Deep standby→Normal In)

ITEM	Modified Driver IC		REMARK
	Register Address	Register Data list	
RESX (RESX ="L")			
WAIT 10ms (min 0ms)			
AVDD+ =5.0V			
WAIT 10ms (min 0ms)			
AVDD-=-5.0V			
WAIT 10ms (min 3ms)			
RESX = H			
Wait 10ms (min 3ms)			
NVM Protect OFF			
Manufacturer Command Access Protect	B0h	04h	
Interface Setting	B3h	**h	04h Command mode 35h Video mode
		00h	Interface setting
		00h	
		22h	
		00h	
		00h	
NVM LOAD	D6h	01h	
Set_pixel_format	3Ah	77h	24 bits/pixel (16,777,216 colors)
Column Address	2Ah	00h 00h 04h 37h	(Only command mode)
Page Address	2Bh	00h 00h 07h 7Fh	(Only command mode)
Set_tear_on	35h	00h	Vsync On (Only command mode)
Display pattern	2C/3C	**	Black pattern (Only command mode)
SLEEP OUT			
SLPOUT	11h	-	
DSI Vedio mode transfer start			
WAIT MIN 120ms			[Automatic] Sleep Mode Off
Display On			
DISPON	29h	-	

BackLight ON			
Write_display_brightness	51h	0x00	0FFh : LED light=100%
		0XFF	
Write_content_adaptive_brightness_control	55h	0x**	CABC OFF=00h CABC ON=02h
Write_control_display (BackLight On)	53h	0x2C	LED(PWM) On
Display pattern			

7. Optical Characteristics

Table 18: IOVDD=1.8 V,AVDD+ =5.0V,AVDD- =-5.0V, ILED=20mA, Ta = 25℃

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Remark
Brightness	L	θ_1=0°	350	450	-	cd/m^2	Note 1, 4
Contrast	CR	θ_1=0°	700	1000	-	-	Note 1, 2,4
Viewing Angle	θ_{11}	CR>10	-	80	-	°(degree)	Note 1, 2
	θ_{12}		-	80	-		
	θ_{21}		-	80	-		
	θ_{22}		-	80	-		
Response Time	Tr+Td	θ_1=0°	-	-	35	ms	Note 1,3
White Chromaticity	x	θ_1=0°	0.27	0.30	0.33	-	Note 1, 4
	y		0.28	0.31	0.34		
Red Chromaticity	x	θ_1=0°	0.64	0.67	0.70	-	Note 1, 4
	y		0.28	0.31	0.34	-	
Green Chromaticity	x	θ_1=0°	0.24	0.27	0.30	-	Note 1, 4
	y		0.60	0.63	0.66	-	
Blue Chromaticity	x	θ_1=0°	0.13	0.16	0.19	-	Note 1, 4
	y		0.03	0.06	0.09	-	
Uniformity	-	θ_1=0°	80	90	-	%	Note1, 5
NTSC ratio	S	θ_1=0°	77	85	-	%	Note 1, 4

*1: Measuring condition

·Temperature = 25℃(±3℃), Frame Frequency =(58Hz), LED back-light: ON, Environment brightness < 150 lx

·Measured sample : New sample before a long term aging.

Brightness/ Contrast/ Chromaticity/Uniformity/ NTSC ratio Test device:SR3,SRUL-2.

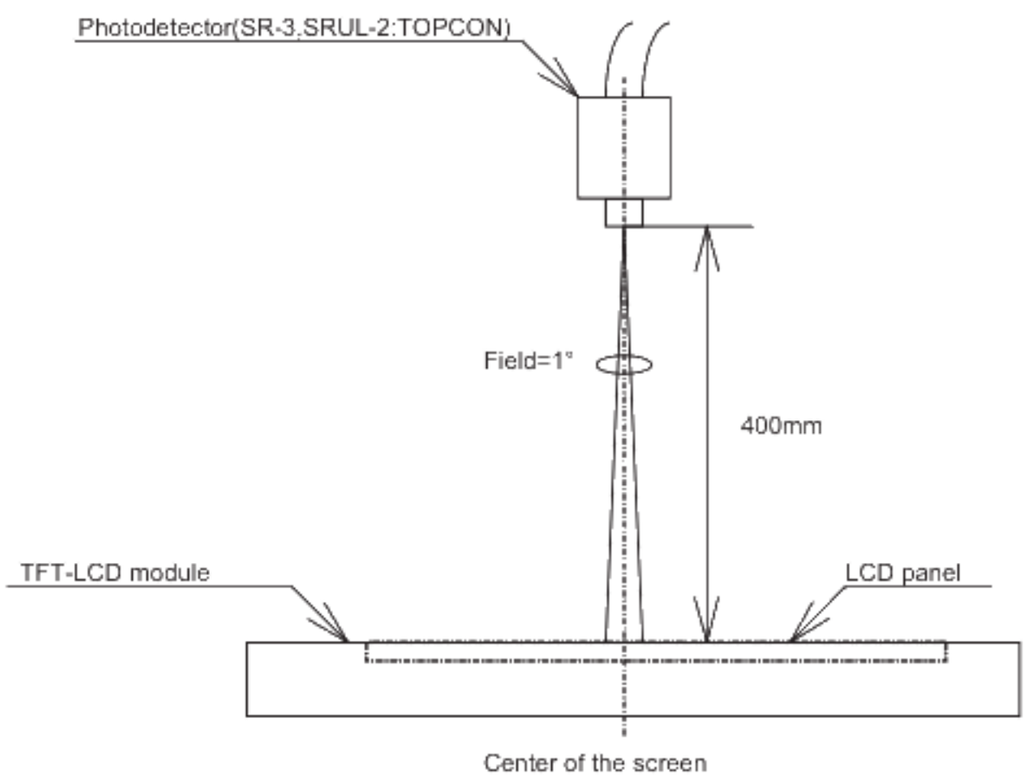


Fig.11 Optical characteristics Test Method(SR3, SRUL-2)

Viewing Angle/ Response Time Test device:DMS
(Note 1) Definition of range of visual angle

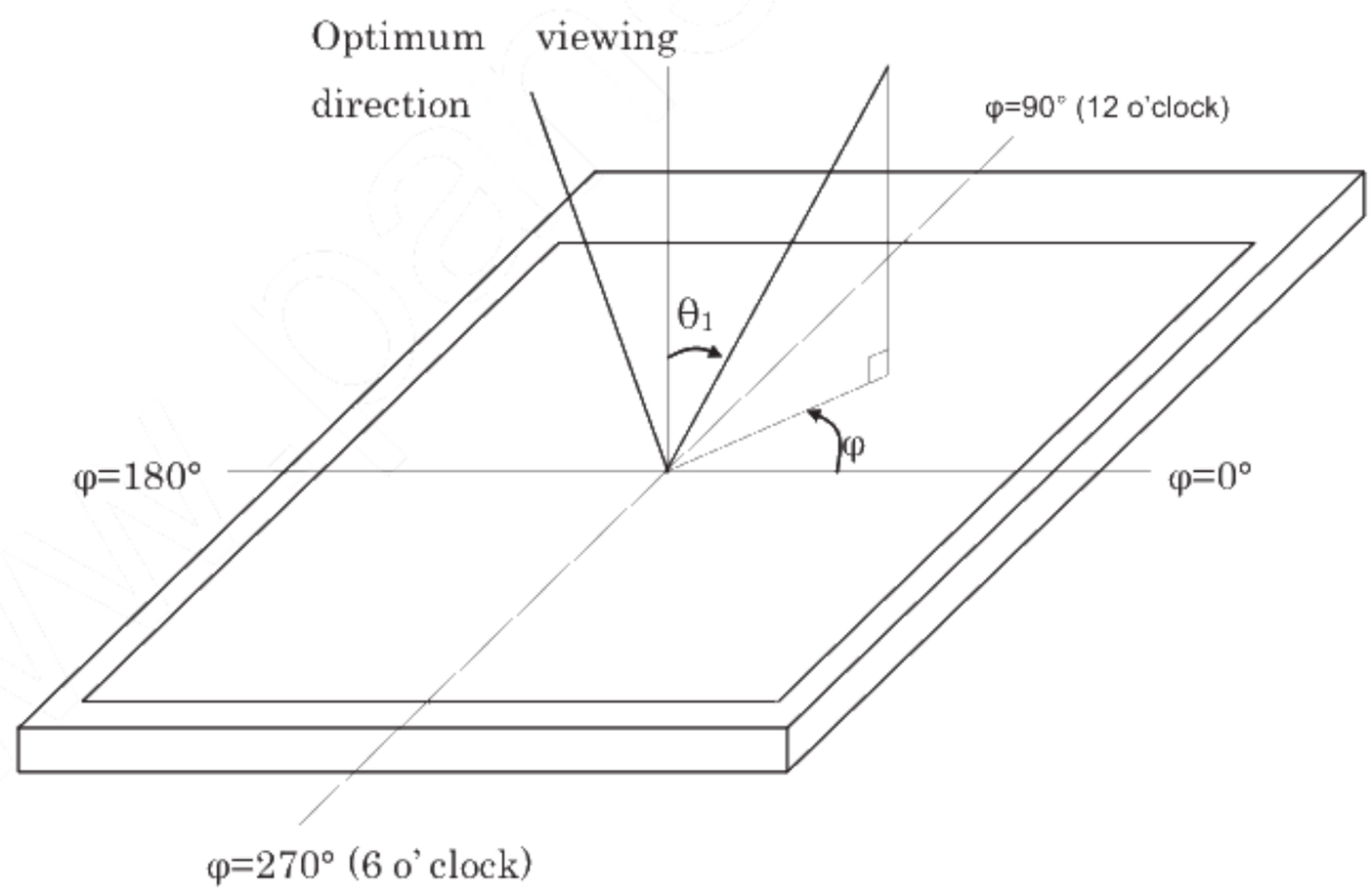


Fig.12 Definition of viewing angle

(Note 2) Contrast ratio is defined as follows:

$$Co = \frac{\text{Luminance(brightness) all pixcels “White”}}{\text{Luminance(brightness) all pixcels “Black”}}$$

(Note 3) Response time is defined as follows:

Definition of response time: The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”

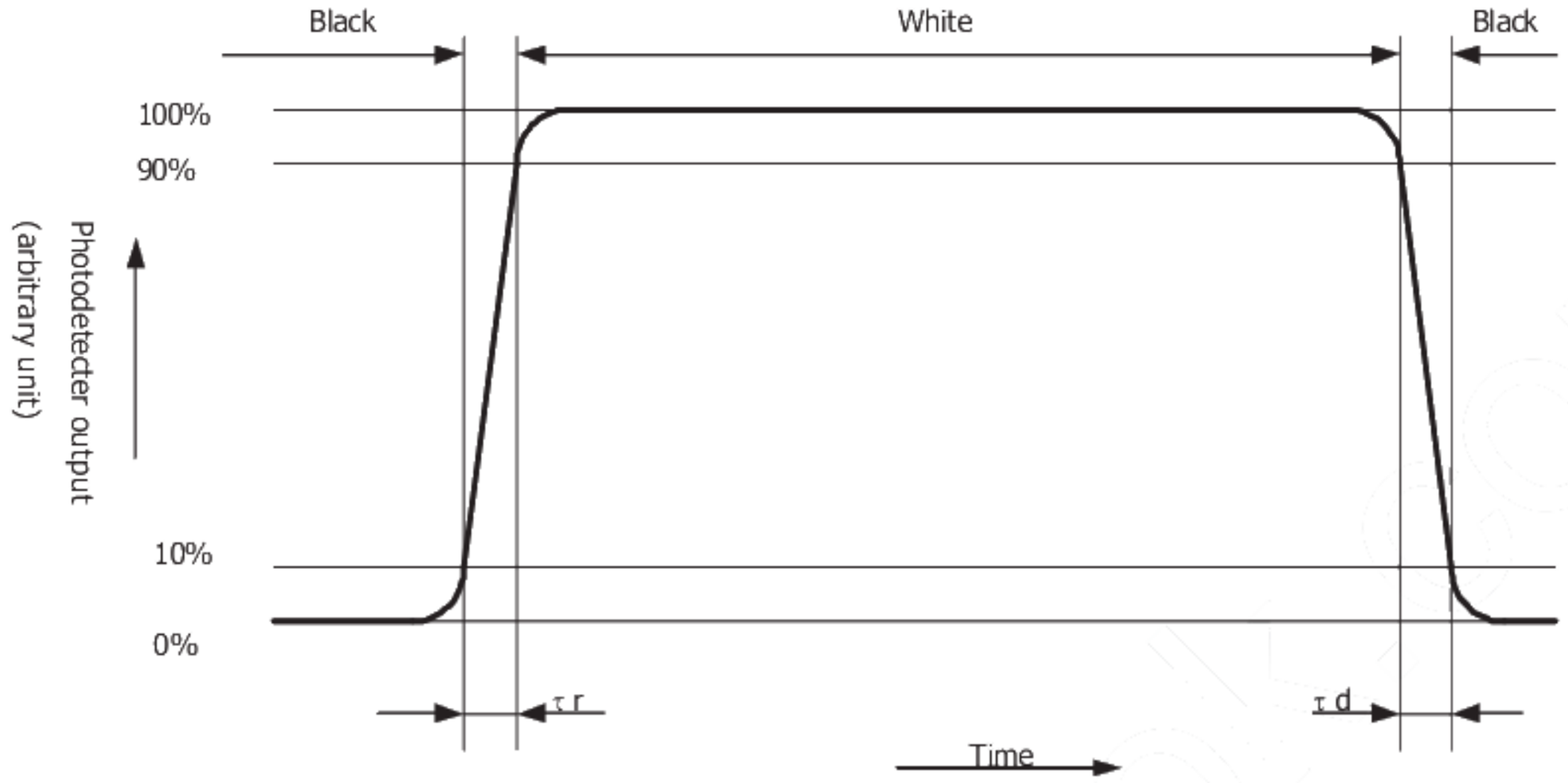


Fig.13 Response time

(Note 4) This shall be measured at center of the screen.

(Note 5) Uniformity is defined as follows:

$$\text{Uniformity} = \frac{\text{Minimum Brightness}}{\text{Maximum Brightness}} \times 100\ [\%]$$

The brightness should be measured on the 9-point as shown in the below figure.

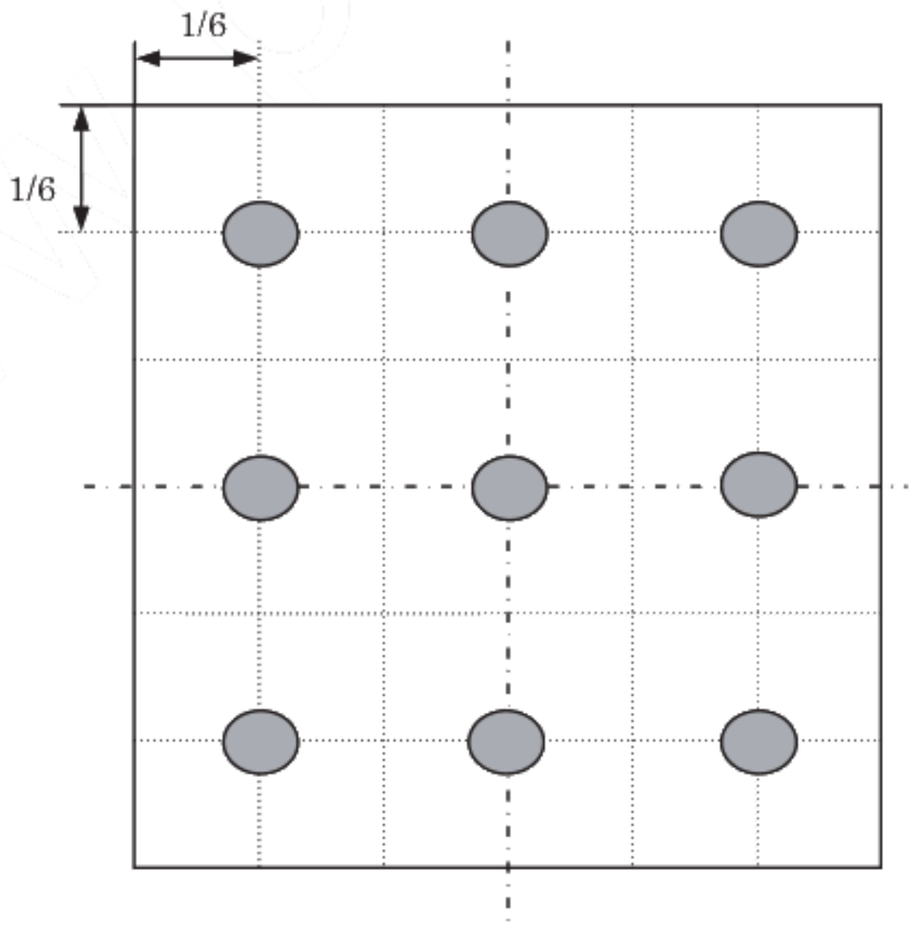


Fig.14 Definition of measurement points

8. Reliability test items

Table 19

No.	Test item	Condition
1	High temperature storage test	Ta = 70°C 240h
2	Low temperature storage test	Ta = -30°C 240h
3	High temperature & high humidity operation test	Ta = 40°C ; 90%RH 240h
4	High temperature operation test	Ta = 60°C 240h
5	Low temperature operation test	Ta = -20°C 240h
6	Thermal shock test (non-operating)	Ta=-30°C to 70°C / 50 cycles 30 min (3 min) 30 min
7	Electro static discharge test	±200V/200pF(0Ω) to Terminals(Contact) (1 time for each terminals)

Table 20

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

9. Packaging specifications

(9-1) Details of packaging

1) Packaging materials: Table25

2) Packaging style : Fig. 15, Fig. 16

(9-2) Reliability

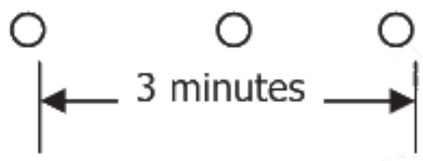
1) Vibration test

Table 21

Item	Test			
Frequency	5 Hz to 50 Hz (3 minutes cycle)			
Direction	Up-Down, Left-Right, Front-Back (3 directions)			
Period	Up-Down	Left-Right	Front-Back	Total
	60min	15min	15min	90min

The frequency should start at 5 Hz and vary continuously.

Total amplitude	20mm	0.2mm	20mm	0.2mm	
Frequency	5 Hz	50 Hz	5 Hz	50 Hz	(For 9.8m/s^2)



2) Drop test

Drop height: 750mm

Number of drop: 10 times (Drop sequence: 1 corner, 3 edges, 6 faces)

(9-3) Packaging quantities

80 modules per master carton

(9-4) Packaging weight

About 7.1Kg

(9-5) Packaging outline dimensions

575 mm×360 mm×225 mm (H)

(Packaging materials)

Table25

	Parts name	CRITERION(after test)
1	Master carton	Corrugate card board
2	Inside sleeve	Corrugate card board
3	Outside sleeve	Corrugate card board
4	Tray for packaging	Polystyrene with anti-static treatment +anti-static polystyrene
5	Protective bag	Polystyrene with anti-static treatment
6	OPP tape	Polypropylene
7	Bar code label	anti-static polystyrene

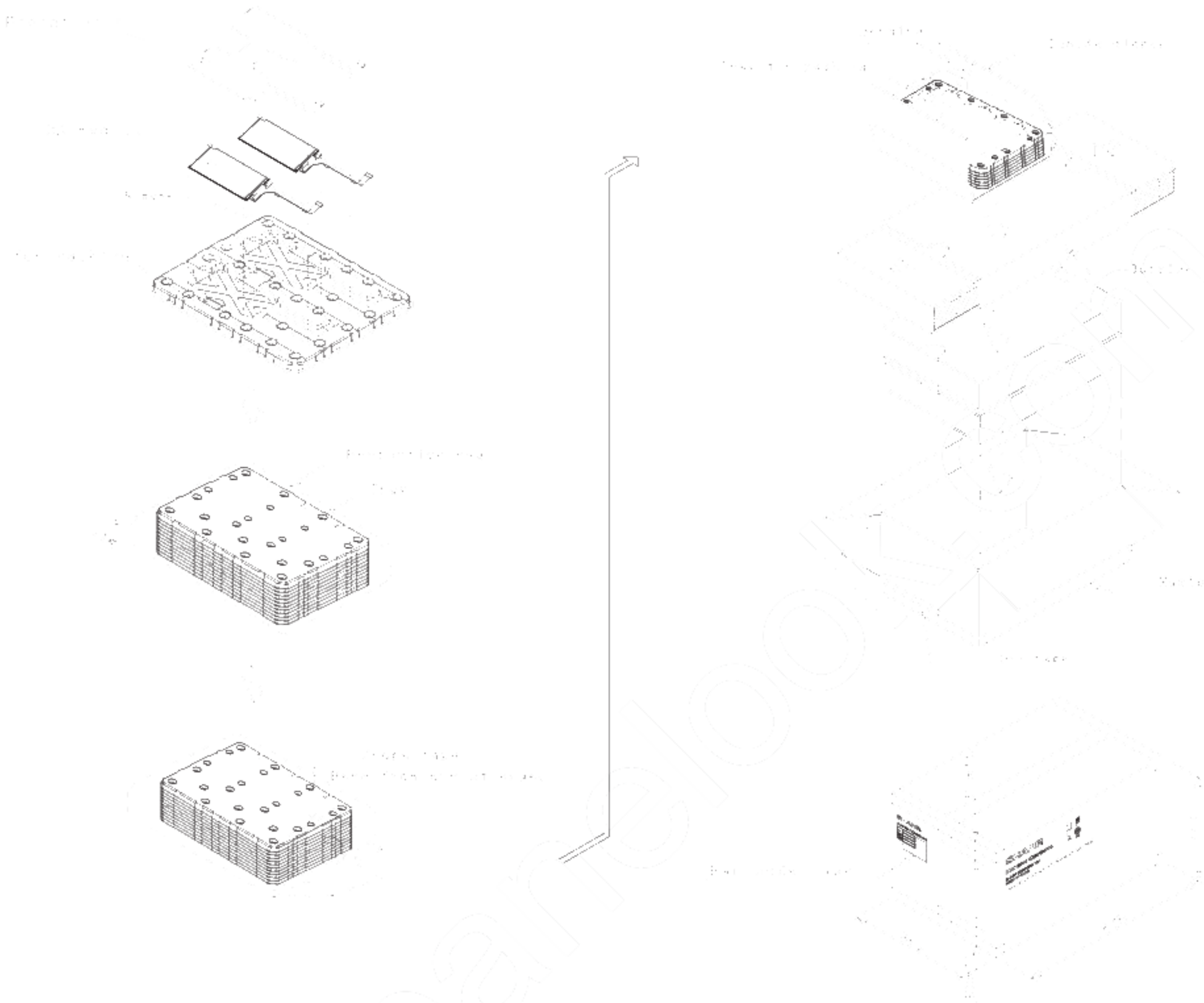


Fig.15 Packaging style (Tray for packaging)

Bar code label

Fig.16 Packaging style (Master carton for packaging)

10. Serial Number Label identification

Numbering is specified as follows.

4 A 000001 A Q

①② ③ ④⑤

① product year (lower 1 digits)

4: 2014

5: 2015

② product month

A: January
B: February
C: March
:
I: September
J: October
K: November
L: December

③ serial number

000001 ~ 999999

④ Version number

⑤ factory code

11. LCD module Outline dimensions

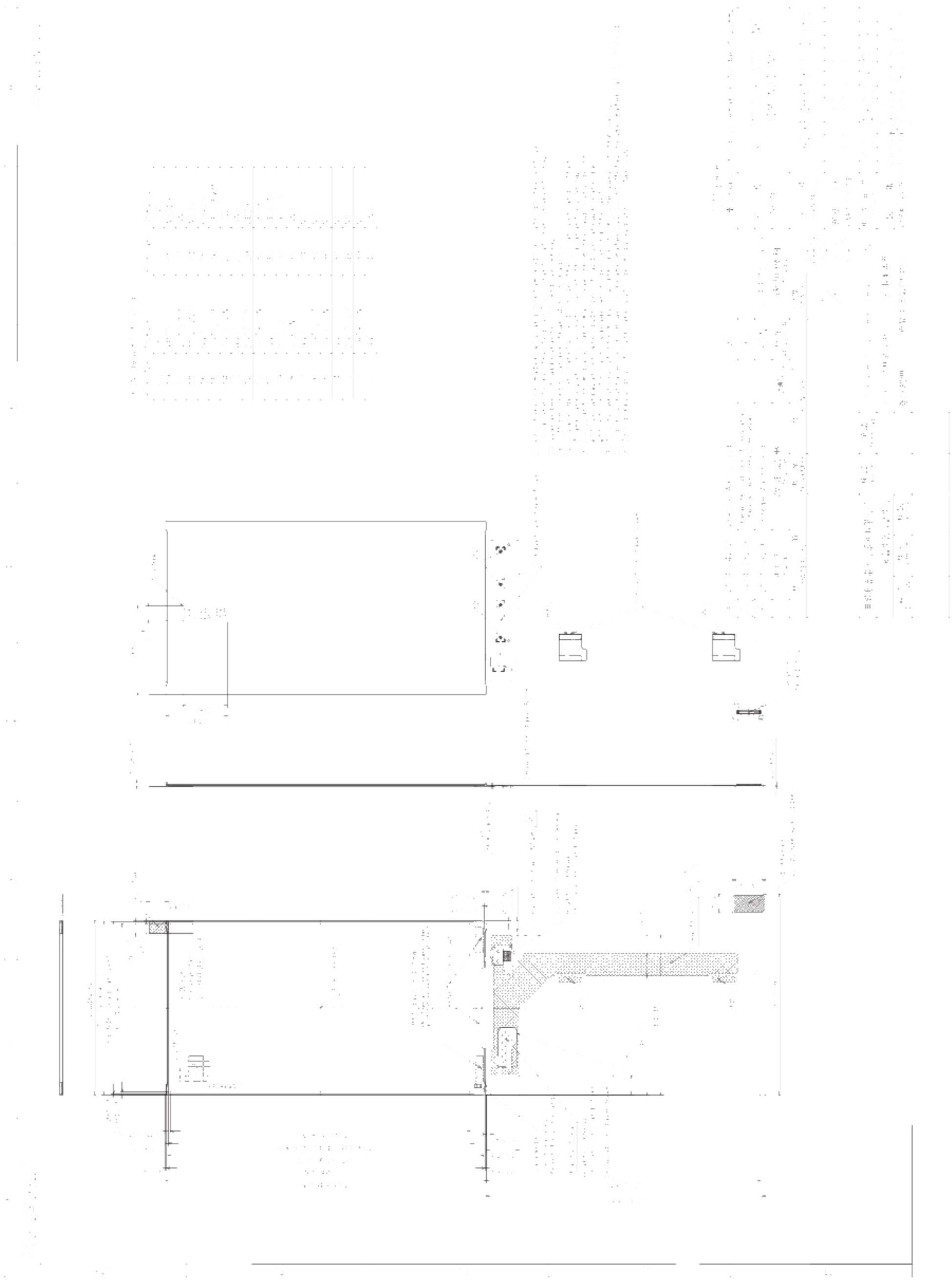


Fig.17 Outline