

TFT COLOR LCD MODULE

NL160120BC27-02

54.0cm (21.3 Type)

UXGA

LVDS Interface (2 ports)

DATA SHEET 

DOD-PD-0266 (1st edition)

**This DATA SHEET is updated document from
PRELIMINARY DATA SHEET DOD-PD-0162(2).**

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INTRODUCTION

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CONTENTS

INTRODUCTION	2
1. OUTLINE	4
1.1 STRUCTURE AND PRINCIPLE.....	4
1.2 APPLICATION	4
1.3 FEATURES.....	4
2. GENERAL SPECIFICATIONS	5
3. BLOCK DIAGRAM	6
4. DETAILED SPECIFICATIONS	7
4.1 MECHANICAL SPECIFICATIONS	7
4.2 ABSOLUTE MAXIMUM RATINGS	7
4.3 ELECTRICAL CHARACTERISTICS	8
4.3.1 LCD panel signal processing board	8
4.3.2 Backlight lamp	9
4.3.3 Power supply voltage ripple.....	10
4.3.4 Fuse	10
4.4 POWER SUPPLY VOLTAGE SEQUENCE	11
4.5 INTERFACING AND PIN ASSIGNMENT OF CONNECTORS	12
4.5.1 Positions of plug and socket	12
4.5.2 LCD panel signal processing board	13
4.5.3 Backlight lamp	15
4.6 DATA INPUT MAP	16
4.6.1 Mode A	16
4.6.2 Mode B	17
4.6.3 Mode C	18
4.7 DISPLAY COLORS AND INPUT DATA SIGNALS	19
4.8 INPUT SIGNAL TIMINGS	20
4.8.1 Timing characteristics	20
4.8.2 Input signal timing chart	20
4.9 DISPLAY POSITIONS.....	21
4.10 TEN-bit LOOK UP TABLE FOR GAMMA ADJUSTMENT.....	22
4.11 LUT SERIAL COMMUNICATION TIMINGS	25
4.11.1 Timing Chart	25
4.11.2 Timing specifications	26
4.12 OPTICS.....	27
4.12.1 Optical characteristics	27
4.12.2 Definition of contrast ratio.....	28
4.12.3 Definition of luminance uniformity	28
4.12.4 Definition of response times	28
4.12.5 Definition of viewing angles.....	28
5. RELIABILITY TESTS.....	29
6. PRECAUTIONS	30
6.1 MEANING OF CAUTION SIGNS	30
6.2 CAUTIONS	30
6.3 ATTENTIONS	30
6.3.1 Handling of the product	30
6.3.2 Environment.....	31
6.3.3 Characteristics.....	31
6.3.4 Other	31
7. OUTLINE DRAWINGS	32
7.1 FRONT VIEW	32
7.2 REAR VIEW	33

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

NL160120BC27-02 module is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a color-filter glass substrate.

Color (Red, Green, Blue) data signals from a host system (e.g. PC, signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Color images are created by regulating the amount of transmitted light through the TFT array of red, green and blue dots.

1.2 APPLICATION

- Monitor for PC

1.3 FEATURES

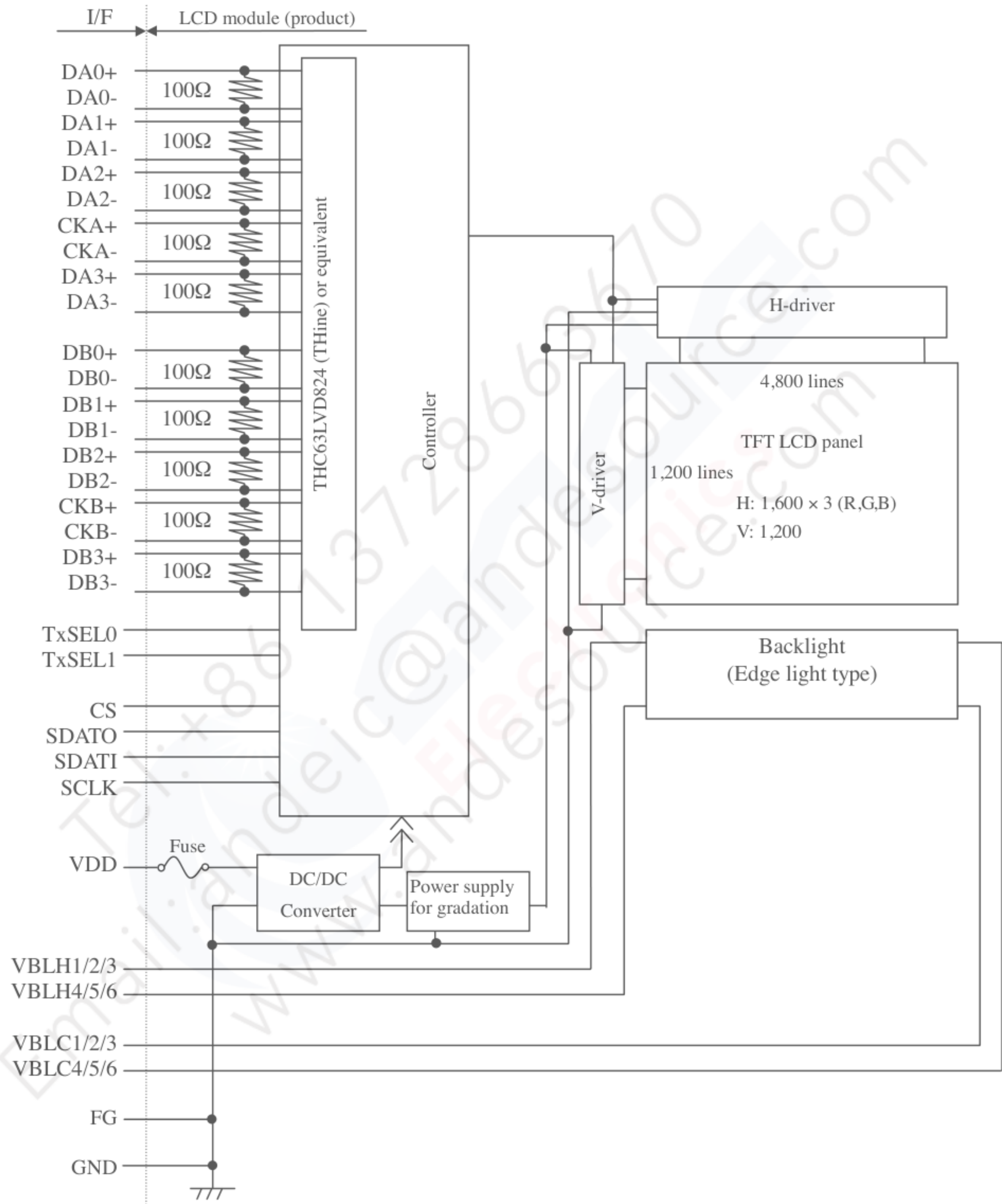
- Ultra-wide viewing angle (with lateral electric field)
- High luminance
- Wide color gamut
- High resolution
- LVDS interface
- Adjustable gamma characteristics by using built-in 10-bit LUT (look up table)
- Selectable LVDS data input map
- Small foot print
- Incorporated edge light type backlight (without inverter)

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2. GENERAL SPECIFICATIONS


<i>Display area</i>	432.0 (H) × 324.0 (V) mm (typ.)
<i>Diagonal size of display</i>	54.0 cm (21.3 inches)
<i>Drive system</i>	a-Si TFT active matrix
<i>Display color</i>	16,777,216 colors
<i>Pixel</i>	1,600 (H) × 1,200 (V) pixels
<i>Pixel arrangement</i>	RGB (Red dot, Green dot, Blue dot) vertical stripe
<i>Dot pitch</i>	0.090 (H) × 0.270 (V) mm
<i>Pixel pitch</i>	0.270 (H) × 0.270 (V) mm
<i>Module size</i>	457.0 (W) × 350.0 (H) × 25.0 (D) mm (typ.)
<i>Weight</i>	3,750 g (typ.)
<i>Contrast ratio</i>	450:1 (typ.)
<i>Viewing angle</i>	At the contrast ratio $\geq 10:1$ • Horizontal: Right side 85° (typ.), Left side 85° (typ.) • Vertical: Up side 85° (typ.), Down side 85° (typ.)
<i>Designed viewing direction</i>	Viewing angle with optimum grayscale ($\gamma=2.2$): normal axis
<i>Polarizer surface</i>	Antiglare
<i>Polarizer pencil-hardness</i>	2H (min.) [by JIS K5400]
<i>Color gamut</i>	At LCD panel center 72% (typ.) [against NTSC color space]
<i>Response time</i>	$T_{on}+T_{off}$ (10% $\longleftrightarrow$ 90%) 20 ms (typ.)
<i>Luminance</i>	At $IBL= 6.0mArms / lamp$ 250 cd/m ² (typ.)
<i>Signal system</i>	2 ports LVDS interface (THC63LVD824 THine Electronics, Inc. or equivalent) RGB 8-bit signals, Data enable signal (DE), Dot clock (CLK)
<i>Power supply voltage</i>	LCD panel signal processing board: 12.0V
<i>Backlight</i>	Edge light type: 6 cold cathode fluorescent lamps (without inverter)
<i>Power consumption</i>	At checkered flag pattern and $IBL= 6.0mArms / lamp$ 30.7 W (typ.)

3. BLOCK DIAGRAM



Note1: Connections between GND (Signal ground), FG (Frame ground) and VBLC (Lamp low voltage terminal) in the LCD module

GND - FG	Connected
GND - VBLC	Not connected
FG - VBLC	Not connected

Note2: GND and FG must be connected to customer equipment's ground, and it is recommended that GND, FG and customer inverter ground are connected together in customer equipment.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	457.0 ±0.5 (W) × 350.0 ±0.5 (H) × 25.0 ± 0.5 (D) Note1	mm
Display area	432.0 (H) × 324.0 (V) Note1	mm
Weight	3,750 (typ.), 4,000 (max.)	g

Note1: See "7. OUTLINE DRAWINGS".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board	VDD	-0.3 to +14.0	V	Ta = 25°C
	Lamp voltage	VBLH	2,000	Vrms	
Input signal voltage		Vi	-0.3 to +2.8	V	Ta = 25°C VDD=12.0V
Storage temperature		Tst	-20 to +60	°C	-
Operating temperature	Front surface	TopF	0 to +55	°C	Note1
	Rear surface	TopR	0 to + 65	°C	Note2
Relative humidity Note3		RH	≤ 95	%	Ta ≤ 40°C
			≤ 85	%	40 < Ta ≤ 50°C
			≤ 70	%	50 < Ta ≤ 55°C
Absolute humidity Note3		AH	≤ 73 Note4	g/m ³	Ta > 55°C
Operating altitude		-	≤ 4,850	m	0°C ≤ Ta ≤ 55°C
Storage altitude		-	≤ 13,600	m	-20°C ≤ Ta ≤ 60°C

Note1: Measured at center of LCD panel surface (including self-heat)

Note2: Measured at center of LCD module's rear shield surface (including self-heat)

Note3: No condensation

Note4: Ta = 55°C, RH = 70%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta = 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Supply voltage		VDD	10.8	12.0	13.2	V	-
Ripple voltage		VRP	-	-	100	mVp-p	for VDD
Differential input Threshold voltage		VTH	-	-	+100	mV	at VCM=1.2V Note1
		VTL	-100	-	-	mV	
Input voltage swing		VI	0	-	2.4	V	-
Terminating resistance		RT	-	100	-	Ω	-
Control signal input threshold voltage	High	VIH	High must be Open.			-	Note2
	Low	VIL	-	-	0.5	V	
Control signal input current	Low	IIL	-10	-	10	μA	
Serial communication signal input threshold voltage	High	V+	-	1.4	1.9	V	Note3
	Low	V-	0.4	0.7	-	V	
	Hysteresis	VH	0.3	-	-	V	
Output signal threshold voltage	High	VOH	1.9	-	-	V	Note4
	Low	VOL	-	-	0.4	V	
Output signal current	High	IOH	-4	-	-	mA	
	Low	IOL	-	-	4	mA	
Supply current		IDD	-	310 Note5	700 Note6	mA	at VDD=12.0V

Note1: Common mode voltage for LVDS driver

Note2: T_xSEL0, T_xSEL1

Note3: CS, SDAT_I, SCLK

Note4: SDAT_O

Note5: Checkered flag pattern (by EIAJ ED-2522)

Note6: Pattern for maximum current

4.3.2 Backlight lamp

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(Ta=25°C, Note1)

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Lamp current	IBL	3.0	6.0	7.0	mArms	at IBL=6.0mArms: L=250cd/m ² (typ.) Note3
Lamp voltage	VBLH	-	750	-	Vrms	Note2, Note3
Lamp starting voltage	VS	1,460	-	-	Vrms	Ta = 0°C Note2, Note3
		1,220	-	-	Vrms	Ta = 25°C Note2, Note3
Oscillation frequency	FO	50	56	60	kHz	Note4

Note1: This product consists of 6 backlight lamps, and these specifications are for each lamp.

Note2: The lamp voltage cycle between lamps should be kept on a same phase. "VS" and "VBLH" are the voltage value between low voltage side (Cold) and high voltage side (Hot).

Note3: The asymmetric ratio of working waveform for lamps (Lamp voltage peak ratio, Lamp current peak ratio and waveform space ratio) should be less than 5 % (See the following figure.). If the waveform is asymmetric, DC (Direct current) element apply into the lamp. In this case, a lamp lifetime may be shortened, because a distribution of a lamp enclosure substance inclines toward one side between low voltage terminal (Cold terminal) and high voltage terminal (Hot terminal).



Pa: Supply voltage/current peak for positive, Pb: Supply voltage/current peak for negative
Sa: Waveform space for positive part, Sb: Waveform space for negative part

Note4: In case "FO" is not the recommended value, beat noise may display on the screen, because of interference between "FO" and "1/th". Recommended value of "FO" is as following.

$$FO = \frac{1}{4} \times \frac{1}{th} \times (2n-1)$$

th: Horizontal cycle period (See "4.8.1 Timing characteristics".)

n: Natural number (1, 2, 3)

4.3.3 Power supply voltage ripple

This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power supply voltage		Ripple voltage (Measure at input terminal of power supply)	Note1	Unit
VDD	12.0 V	≤ 100		mVp-p

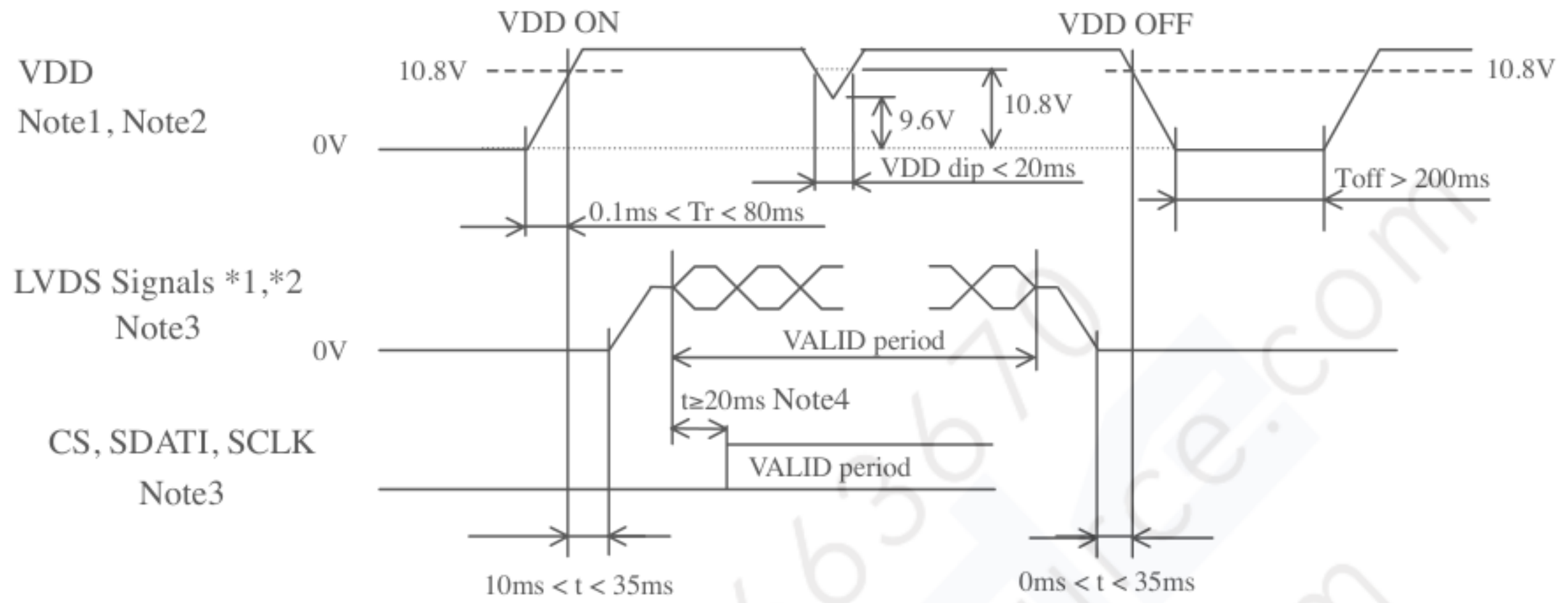
Note1: The permissible ripple voltage includes spike noise.

4.3.4 Fuse

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	FCC16132AB	KAMAYA ELECTRIC Co., Ltd.	1.25 A	2.5 A	Note1
			32V		

Note1: The power supply capacity should be more than the fusing current. If the power supply capacity is less than the fusing current, the fuse may not blow for a short time, and then nasty smell, smoking and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE



*1: LVDS signals: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/- and CKB+/-

*2: LVDS signals should be measured at the terminal of 100Ω resistance.

Note1: In terms of voltage variation (voltage drop) while VDD rising edge is below 10.8V, a protection circuit may work, and then this product may not work.

Note2: VDD should be 10.8V or more while VDD ON period.

Note3: LVDS signals and CS, SDAT1, SCLK must be Low or High-impedance, exclude the VALID period (See above sequence diagram), in order to avoid that internal circuits is damaged.

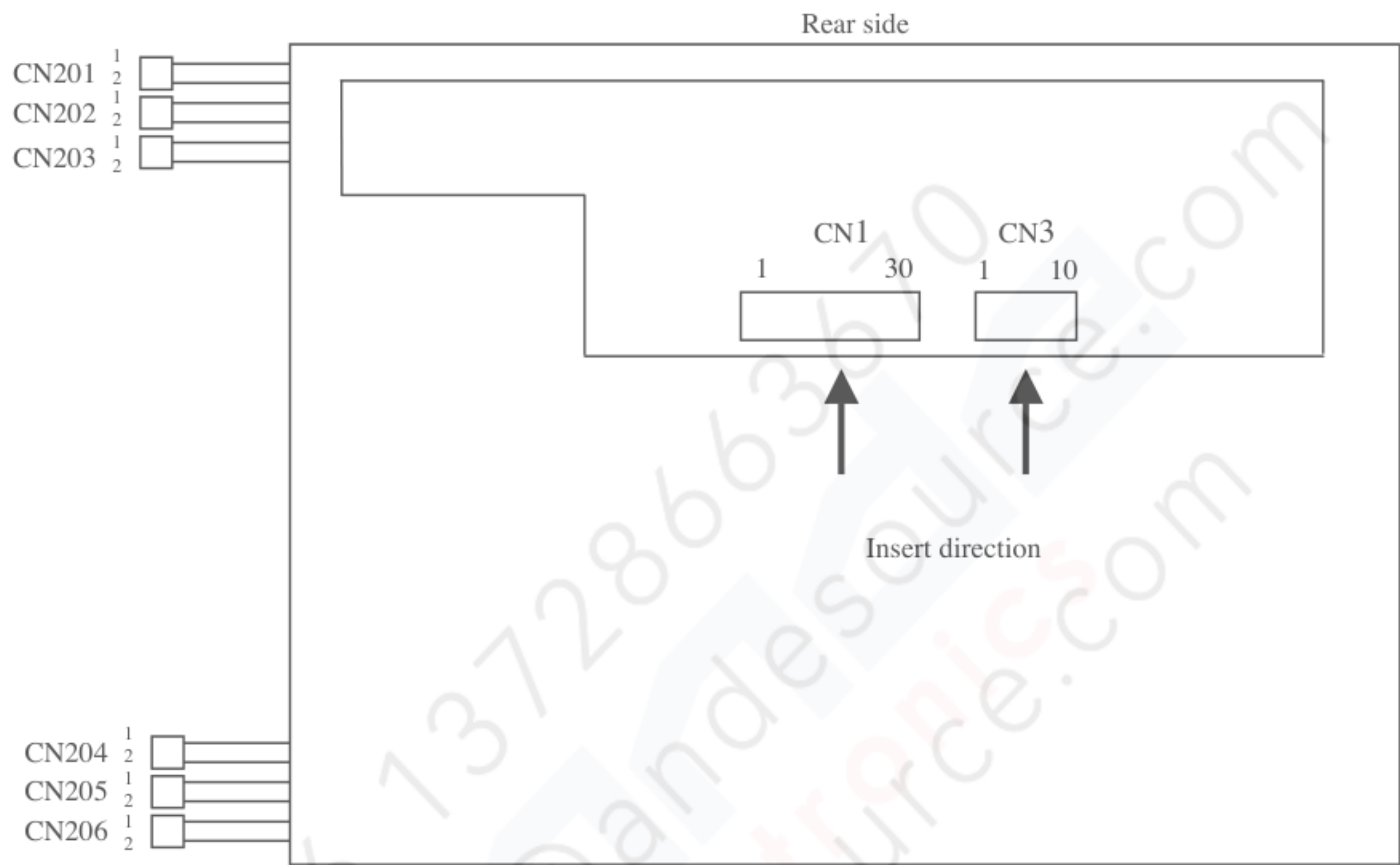
If some of signals are cut while this product is working, even if the signal input to it once again, it might not work normally. If customer stops the display and function signals, they should be cut VDD.

Note4: At the beginning of the serial communication mode, take 20ms or more after the LVDS signal input. When writing and reading the LUT data, see “**4.10 TEN-bit LOOK UP TABLE FOR GAMMA ADJUSTMENT**”.

Note5: The backlight inverter voltage should be inputted within the valid period of LVDS signals, in order to avoid unstable data display.

4.5 INTERFACING AND PIN ASSIGNMENT OF CONNECTORS

4.5.1 Positions of plug and socket



4.5.2 LCD panel signal processing board

(1) CN1

Socket (LCD module side): DF19G-30P-1H (59)/ DF19G-30P-1H (99) (Hirose Electric Co., Ltd.)

Adaptable plug: DF19-30S-1C (Hirose Electric Co., Ltd.)

Pin No.	Symbol	Signal	Remarks				
1	DA0-	Pixel data A0	Odd pixel data Input (LVDS differential signal)		Note1		
2	DA0+						
3	DA1-	Pixel data A1	Odd pixel data Input (LVDS differential signal)		Note1		
4	DA1+						
5	DA2-	Pixel data A2	Odd pixel data Input (LVDS differential signal)		Note1		
6	DA2+						
7	GND	Ground	Signal ground				
8	CKA-	Pixel clock	Odd pixel clock Input (LVDS differential signal)		Note1		
9	CKA+						
10	DA3-	Pixel data A3	Odd pixel data Input (LVDS differential signal)		Note1		
11	DA3+						
12	DB0-	Pixel data B0	Even pixel data Input (LVDS differential signal)		Note1		
13	DB0+						
14	GND	Ground	Signal ground				
15	DB1-	Pixel data B1	Even pixel data Input (LVDS differential signal)		Note1		
16	DB1+						
17	GND	Ground	Signal ground				
18	DB2-	Pixel data B2	Even pixel data Input (LVDS differential signal)		Note1		
19	DB2+						
20	CKB-	Pixel clock	Even pixel clock Input (LVDS differential signal)		Note1		
21	CKB+						
22	DB3-	Pixel data B3	Even pixel data Input (LVDS differential signal)		Note1		
23	DB3+						
24	GND	Ground	Signal ground				
25	TxSEL0	Selection of LVDS data input map	Note2, Note3	TxSEL1		TxSEL0	Mode
26	TxSEL1			Open	Open	A	
				Open	Low	B	
				Low	Open	C	
				Low	Low	A	
27	GND	Ground	Signal ground				
28	VDD	Power supply	12V				
29	VDD	Power supply	12V				
30	VDD	Power supply	12V				

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be connected between LCD panel signal processing board and LVDS transmitter.

Note2: This terminal is pulled-up in the product.

Note3: See "4.6 DATA INPUT MAP".

(2) CN3

Socket (LCD module side): SM10B-SRSS-TB (J.S.T. Mfg Co., Ltd.)

Adaptable plug: SHR-10V-S, SHR-10V-S-B, 10SR-3S (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	RSVD	Reserved	Keep open
2	RSVD	Reserved	Keep open
3	RSVD	Reserved	Keep open
4	GND	Ground	Signal ground
5	CS	Chip selection	For LUT communication control
6	SDATO	Serial data output	For LUT output signal
7	SDATI	Serial data input	For LUT communication control
8	SCLK	Serial clock	For LUT communication control
9	GND	Ground	Signal ground
10	RSVD	Reserved	Keep open

4.5.3 Backlight lamp

Attention: VBLH and VBLC must be connected correctly. If customer connects wrongly, customer will be hurt and the module will be broken.

(1)CN201

Plug (Module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)

Adaptable socket: SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH1	Upper side lamp, High voltage (Hot)	Cable color: Pink
2	VBLC1	Upper side lamp, Low voltage (Cold)	Cable color: Gray

(2)CN202

Plug (Module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)

Adaptable socket: SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH2	Upper side lamp, High voltage (Hot)	Cable color: White
2	VBLC2	Upper side lamp, Low voltage (Cold)	Cable color: Gray

(3)CN203

Plug (Module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)

Adaptable socket: SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH3	Upper side lamp, High voltage (Hot)	Cable color: Red
2	VBLC3	Upper side lamp, Low voltage (Cold)	Cable color: Gray

(4)CN204

Plug (Module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)

Adaptable socket: SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH4	Lower side lamp, High voltage (Hot)	Cable color: Pink
2	VBLC4	Lower side lamp, Low voltage (Cold)	Cable color: Gray

(5)CN205

Plug (Module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)

Adaptable socket: SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH5	Lower side lamp, High voltage (Hot)	Cable color: White
2	VBLC5	Lower side lamp, Low voltage (Cold)	Cable color: Gray

(6)CN206

Plug (Module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)

Adaptable socket: SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH6	Lower side lamp, High voltage (Hot)	Cable color: Red
2	VBLC6	Lower side lamp, Low voltage (Cold)	Cable color: Gray

4.6 DATA INPUT MAP

4.6.1 Mode A

Input data		Transmitter				I/F		THC63LVD824 or equivalent				
		Pin	THC63LVDF83A	Pin	THC63LVD823							
Odd pixel data and control signal	RA2	→	51	TA0	53	R12	Note2	Pin	CN1	→		
	RA3	→	52	TA1	54	R13		1	DA0-		RA-1	
	RA4	→	54	TA2	57	R14	TA1-	→	2	DA0+	RA+1	
	RA5	→	55	TA3	58	R15	TA1+	→				
	RA6	→	56	TA4	59	R16	TB1-	→	3	DA1-	RB-1	
	RA7	→	3	TA5	60	R17	TB1+	→	4	DA1+	RB+1	
	GA2	→	4	TA6	63	G12	TC1-	→	5	DA2-	RC-1	
	GA3	→	6	TB0	64	G13	TC1+	→	6	DA2+	RC+1	
	GA4	→	7	TB1	65	G14	TCLK1-	→	7	GND		
	GA5	→	11	TB2	66	G15	TCLK1+	→	8	CKA-	RCLK-1	
	GA6	→	12	TB3	67	G16		→	9	CKA+	RCLK+1	
	GA7	→	14	TB4	68	G17						
	BA2	→	15	TB5	73	B12	TD1-	→	10	DA3-	RD-1	
	BA3	→	19	TB6	74	B13	TD1+	→	11	DA3+	RD+1	
	BA4	→	20	TC0	75	B14						
	BA5	→	22	TC1	76	B15						
	BA6	→	23	TC2	77	B16						
	BA7	→	24	TC3	78	B17						
	Note1 RSVD	→	27	TC4	7	RSVD						
	Note1 RSVD	→	28	TC5	8	RSVD						
	DE	→	30	TC6	9	DE						
	RA0	→	50	TD0	51	R10						
	RA1	→	2	TD1	52	R11						
	GA0	→	8	TD2	61	G10						
	GA1	→	10	TD3	62	G11						
	BA0	→	16	TD4	69	B10						
	BA1	→	18	TD5	70	B11						
	Note1 RSVD	→	25	TD6	-							
	CLK	→	31	CLKIN	10	CLK						
Even pixel data	RB2	→	51	TA0	81	R22	TA2-	→	12	DB0-	→	RA-2
	RB3	→	52	TA1	82	R23	TA2+	→	13	DB0+	→	RA+2
	RB4	→	54	TA2	83	R24			14	GND		
	RB5	→	55	TA3	84	R25	TB2-	→	15	DB1-	→	RB-2
	RB6	→	56	TA4	85	R26	TB2+	→	16	DB1+	→	RB+2
	RB7	→	3	TA5	86	R27	TC2-	→	17	GND		
	GB2	→	4	TA6	91	G22	TC2+	→	18	DB2-	→	RC-2
	GB3	→	6	TB0	92	G23			19	DB2+	→	RC+2
	GB4	→	7	TB1	93	G24	TCLK2-	→	20	CKB-	→	RCLK-2
	GB5	→	11	TB2	94	G25	TCLK2+	→	21	CKB+	→	RCLK+2
	GB6	→	12	TB3	95	G26						
	GB7	→	14	TB4	96	G27	TD2-	→	22	DB3-	→	RD-2
	BB2	→	15	TB5	99	B22	TD2+	→	23	DB3+	→	RD+2
	BB3	→	19	TB6	100	B23			24	GND		
	BB4	→	20	TC0	1	B24			25	TxSEL0	→	TxSEL0
	BB5	→	22	TC1	2	B25			26	TxSEL1	→	TxSEL1
	BB6	→	23	TC2	5	B26			27	GND		
	BB7	→	24	TC3	6	B27			28	VDD		
	Note1 RSVD	→	27	TC4	-				29	VDD		
	Note1 RSVD	→	28	TC5	-				30	VDD		
	DE	→	30	TC6	-							
	RB0	→	50	TD0	79	R20						
	RB1	→	2	TD1	80	R21						
	GB0	→	8	TD2	89	G20						
	GB1	→	10	TD3	90	G21						
	BB0	→	16	TD4	97	B20						
	BB1	→	18	TD5	98	B21						
	Note1 RSVD	→	25	TD6	-							
	CLK	→	31	CLKIN	-							

4.6.2 Mode B



Input data		Transmitter		I/F		THC63LVD824 or equivalent				
		Pin	DS90CF383, C385							
Odd pixel data and control signal	RA7	→	51	TXIN0	Note2	Pin	CN1			
	RA6	→	52	TXIN1	TA1- →	1	DA0-	→	RA-1	
	RA5	→	54	TXIN2	TA1+ →	2	DA0+	→	RA+1	
	RA4	→	55	TXIN3						
	RA3	→	56	TXIN4	TB1- →	3	DA1-	→	RB-1	
	RA2	→	3	TXIN6	TB1+ →	4	DA1+	→	RB+1	
	GA7	→	4	TXIN7						
	GA6	→	6	TXIN8	TC1- →	5	DA2-	→	RC-1	
	GA5	→	7	TXIN9	TC1+ →	6	DA2+	→	RC+1	
	GA4	→	11	TXIN12		7	GND			
	GA3	→	12	TXIN13	TCLK1- →	8	CKA-	→	RCLK-1	
	GA2	→	14	TXIN14	TCLK1+ →	9	CKA+	→	RCLK+1	
	BA7	→	15	TXIN15						
	BA6	→	19	TXIN18	TD1- →	10	DA3-	→	RD-1	
	BA5	→	20	TXIN19	TD1+ →	11	DA3+	→	RD+1	
	BA4	→	22	TXIN20						
	BA3	→	23	TXIN21						
	BA2	→	24	TXIN22						
	Note1 RSVD	→	27	TXIN24						
	Note1 RSVD	→	28	TXIN25						
	DE	→	30	TXIN26						
	RA1	→	50	TXIN27						
	RA0	→	2	TXIN5						
	GA1	→	8	TXIN10						
	GA0	→	10	TXIN11						
	BA1	→	16	TXIN16						
	BA0	→	18	TXIN17						
	Note1 RSVD	→	25	TXIN23						
	CLK	→	31	CLKIN						
	Even pixel data	RB7	→	51	TXIN0					
		RB6	→	52	TXIN1	TA2- →	12	DB0-	→	RA-2
RB5		→	54	TXIN2	TA2+ →	13	DB0+	→	RA+2	
RB4		→	55	TXIN3		14	GND			
RB3		→	56	TXIN4	TB2- →	15	DB1-	→	RB-2	
RB2		→	3	TXIN6	TB2+ →	16	DB1+	→	RB+2	
GB7		→	4	TXIN7		17	GND			
GB6		→	6	TXIN8	TC2- →	18	DB2-	→	RC-2	
GB5		→	7	TXIN9	TC2+ →	19	DB2+	→	RC+2	
GB4		→	11	TXIN12						
GB3		→	12	TXIN13	TCLK2- →	20	CKB-	→	RCLK-2	
GB2		→	14	TXIN14	TCLK2+ →	21	CKB+	→	RCLK+2	
BB7		→	15	TXIN15						
BB6		→	19	TXIN18	TD2- →	22	DB3-	→	RD-2	
BB5		→	20	TXIN19	TD2+ →	23	DB3+	→	RD+2	
BB4		→	22	TXIN20		24	GND			
BB3		→	23	TXIN21		25	TxSEL0	→	TxSEL0	
BB2		→	24	TXIN22		26	TxSEL1	→	TxSEL1	
Note1 RSVD		→	27	TXIN24		27	GND			
Note1 RSVD		→	28	TXIN25		28	VDD			
DE		→	30	TXIN26		29	VDD			
RB1		→	50	TXIN27		30	VDD			
RB0		→	2	TXIN5						
GB1		→	8	TXIN10						
GB0		→	10	TXIN11						
BB1		→	16	TXIN16						
BB0		→	18	TXIN18						
Note1 RSVD		→	25	TXIN23						
CLK		→	31	CLKIN						

4.6.3 Mode C



Input data		Transmitter		I/F		THC63LVD824					
		Pin	DS90CF383, C385			Pin	CN1	or equivalent			
Odd pixel data and control signal	RA0	→	51 TXIN0	Note2	TA1-	→	1 DA0-	→	RA-1		
	RA1	→	52 TXIN1		TA1+	→	2 DA0+	→	RA+1		
	RA2	→	54 TXIN2								
	RA3	→	55 TXIN3								
	RA4	→	56 TXIN4		TB1-	→	3 DA1-	→	RB-1		
	RA5	→	3 TXIN6		TB1+	→	4 DA1+	→	RB+1		
	GA0	→	4 TXIN7								
	GA1	→	6 TXIN8		TC1-	→	5 DA2-	→	RC-1		
	GA2	→	7 TXIN9		TC1+	→	6 DA2+	→	RC+1		
	GA3	→	11 TXIN12				7 GND				
	GA4	→	12 TXIN13		TCLK1-	→	8 CKA-	→	RCLK-1		
	GA5	→	14 TXIN14		TCLK1+	→	9 CKA+	→	RCLK+1		
	BA0	→	15 TXIN15								
	BA1	→	19 TXIN18		TD1-	→	10 DA3-	→	RD-1		
	BA2	→	20 TXIN19		TD1+	→	11 DA3+	→	RD+1		
	BA3	→	22 TXIN20								
	BA4	→	23 TXIN21								
	BA5	→	24 TXIN22								
	Note1 RSVD	→	27 TXIN24								
	Note1 RSVD	→	28 TXIN25								
	DE	→	30 TXIN26								
	RA6	→	50 TXIN27								
	RA7	→	2 TXIN5								
	GA6	→	8 TXIN10								
	GA7	→	10 TXIN11								
	BA6	→	16 TXIN16								
	BA7	→	18 TXIN17								
	Note1 RSVD	→	25 TXIN23								
	CLK	→	31 CLKIN								
	Even pixel data	RB0	→		51 TXIN0	Note2	TA2-	→	12 DB0-	→	RA-2
		RB1	→		52 TXIN1		TA2+	→	13 DB0+	→	RA+2
RB2		→	54 TXIN2				14 GND				
RB3		→	55 TXIN3								
RB4		→	56 TXIN4	TB2-	→		15 DB1-	→	RB-2		
RB5		→	3 TXIN6	TB2+	→		16 DB1+	→	RB+2		
GB0		→	4 TXIN7				17 GND				
GB1		→	6 TXIN8	TC2-	→		18 DB2-	→	RC-2		
GB2		→	7 TXIN9	TC2+	→		19 DB2+	→	RC+2		
GB3		→	11 TXIN12								
GB4		→	12 TXIN13	TCLK2-	→		20 CKB-	→	RCLK-2		
GB5		→	14 TXIN14	TCLK2+	→		21 CKB+	→	RCLK+2		
BB0		→	15 TXIN15								
BB1		→	19 TXIN18	TD2-	→		22 DB3-	→	RD-2		
BB2		→	20 TXIN19	TD2+	→		23 DB3+	→	RD+2		
BB3		→	22 TXIN20				24 GND				
BB4		→	23 TXIN21				25 TxSEL0	→	TxSEL0		
BB5		→	24 TXIN22				26 TxSEL1	→	TxSEL1		
Note1 RSVD		→	27 TXIN24				27 GND				
Note1 RSVD		→	28 TXIN25				28 VDD				
DE		→	30 TXIN26				29 VDD				
RB6		→	50 TXIN27				30 VDD				
RB7		→	2 TXIN5								
GB6		→	8 TXIN10								
GB7		→	10 TXIN11								
BB6		→	16 TXIN16								
BB7		→	18 TXIN18								
Note1 RSVD		→	25 TXIN23								
CLK		→	31 CLKIN								

Note1: Input signal RSVD is not used inside the product, but do not keep this pin open to avoid noise problem.

☆

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be connected between LCD panel signal processing board and LVDS transmitter.

4.7 DISPLAY COLORS AND INPUT DATA SIGNALS

This product can display in equivalent to 16,777,216 colors in 256 scale. Also the relation between display colors and input data signals is as the following table.

Display colors		Data signal (0: Low level, 1: High level)																							
		RA7 RA6 RA5 RA4 RA3 RA2 RA1 RA0								GA7 GA6 GA5 GA4 GA3 GA2 GA1 GA0								BA7 BA6 BA5 BA4 BA3 BA2 BA1 BA0							
		RB7 RB6 RB5 RB4 RB3 RB2 RB1 RB0								GB7 GB6 GB5 GB4 GB3 GB2 GB1 GB0								BB7 BB6 BB5 BB4 BB3 BB2 BB1 BB0							
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑																								
	↓																								
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Green grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	↑																								
	↓																								
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Blue grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	↑																								
	↓																								
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0
Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

4.8 INPUT SIGNAL TIMINGS

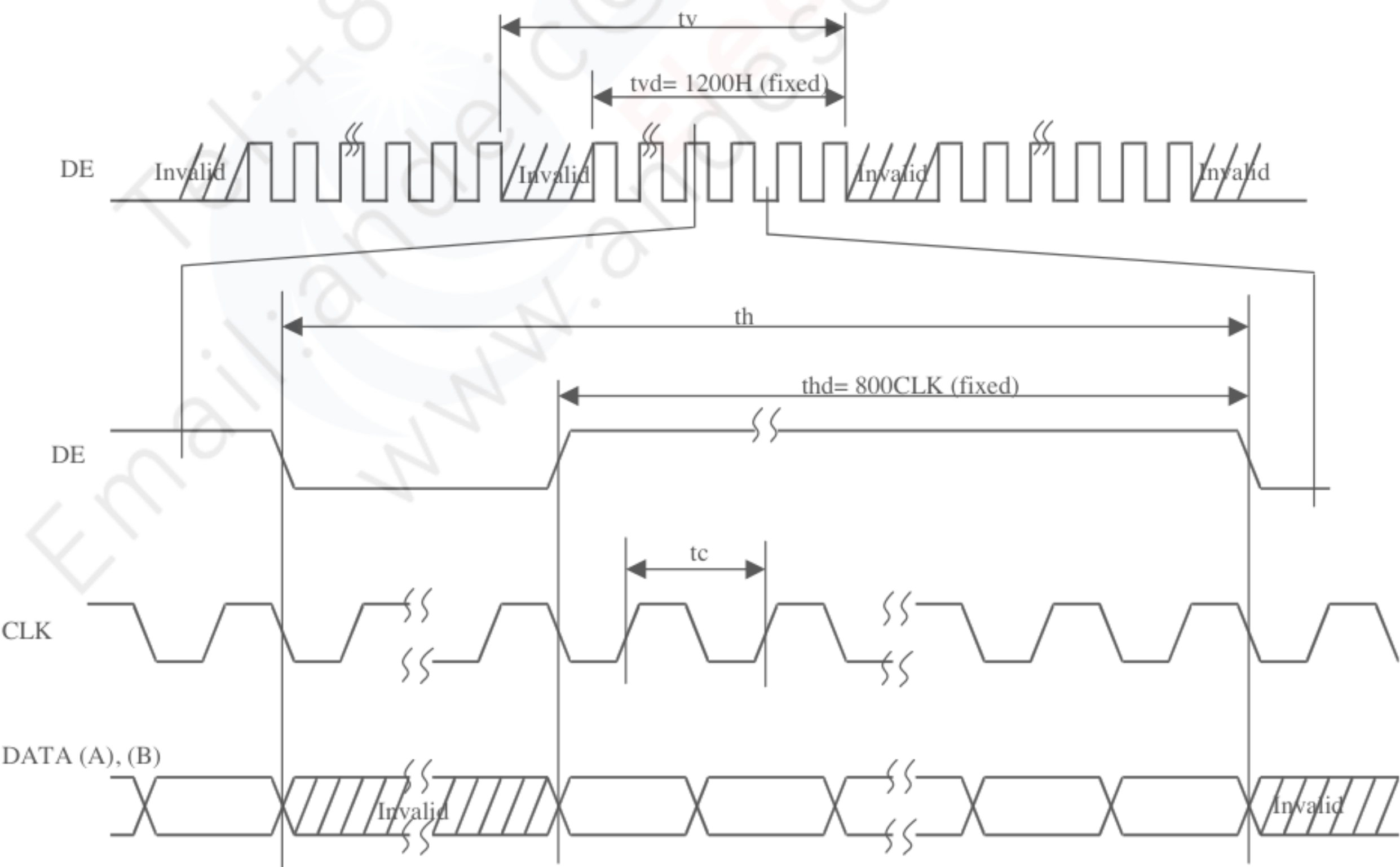
4.8.1 Timing characteristics



Parameter		Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency	1/ tc	60.0	62.5	65.0	MHz	LVDS transmitter input
	Pulse width	tc	15.38	16.0	-	ns	
	Duty	-	See the data sheet of LVDS transmitter.			-	-
	Rise, fall	-				ns	
Horizontal	Cycle period	th	-	13.3	-	μs	Note1
			848	1,080	1,156	CLK	
	Display period	thd	800			CLK	-
Vertical	Cycle period	1/tv	59	60	61	Hz	-
		tv	1,206	1,250	-	H	
	Display period	tvd	1,200			H	-
DE, DATA	Setup time	-	See the data sheet of LVDS transmitter.			ns	-
	Hold time	-				ns	
	Rise, fall	-				ns	

Note1: During operation, fluctuation of horizontal cycle period must not exceed ± 1 CLK. Otherwise function errors will occur in LCD module.
e.g.: Acceptable fluctuation range is 1,079-1,081 CLK, when the horizontal cycle period is 1,080 CLK.

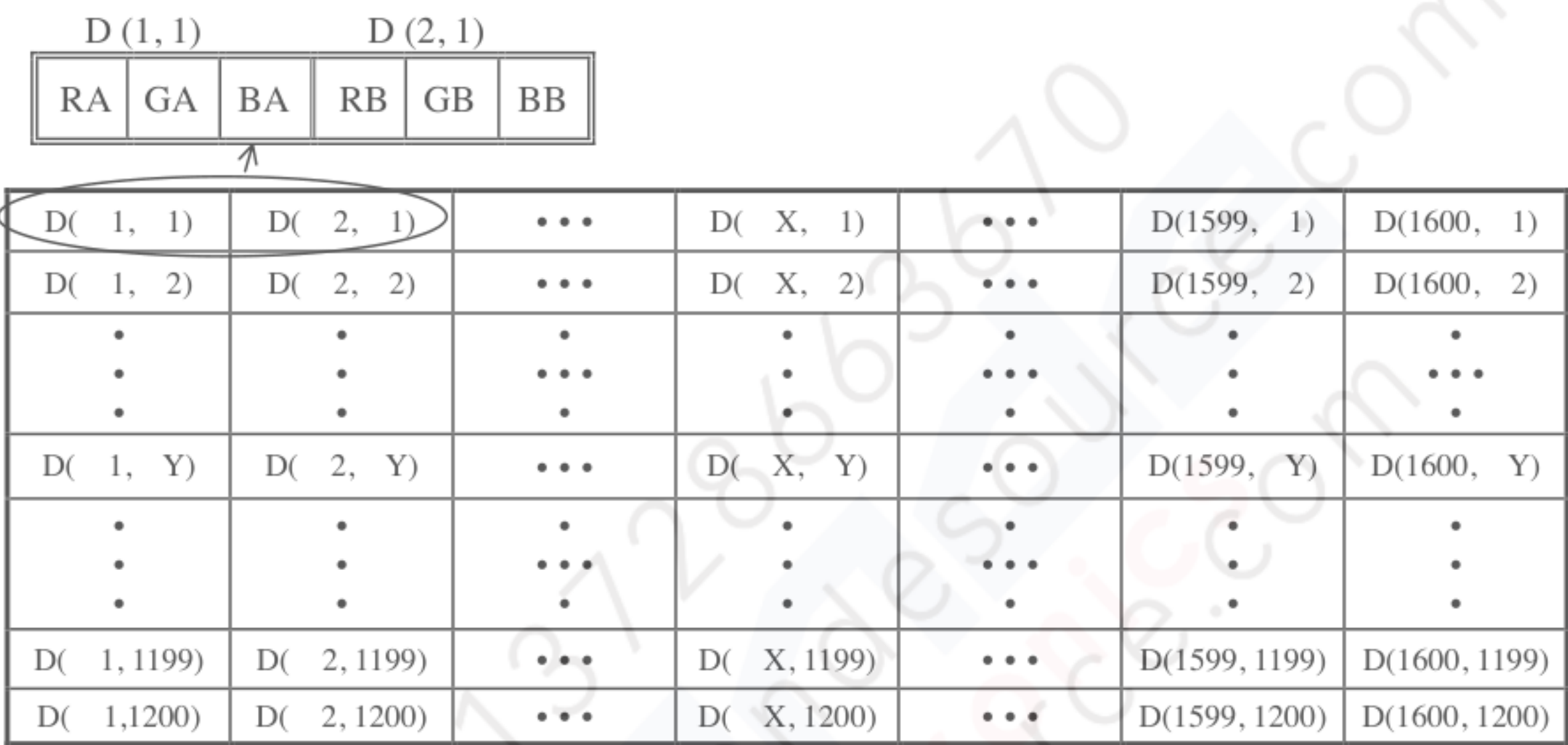
4.8.2 Input signal timing chart



4.9 DISPLAY POSITIONS

Odd pixel: RA= Red data
 GA= Green data
 BA= Blue data

Even pixel: RB= Red data
 GB= Green data
 BB= Blue data



4.10 TEN-bit LOOK UP TABLE FOR GAMMA ADJUSTMENT

Adjustment of gamma characteristics for each 8-bit RGB color data is possible by using built-in 10-bit LUT (look up table) for Gamma characteristics.

The LUT is set with the serial data. The combination of the control command determines the R/W actions.:
READ, Random/Sequential Address WRITE and Individual/Simultaneous RGB setting.

The serial data is composed as Table 1.

Table1: Serial data Composition

DATA	DATA name	Function	Remarks
D31	CMD5	Control Command	See Table2 and 3.
D30	CMD4	Control Command	
D29	CMD3	Control Command	
D28	CMD2	Control Command	
D27	CMD1	Control Command	
D26	CMD0	Control Command	
D25	ADD9	LUT Address (MSB)	See Table4.
D24	ADD8	LUT Address	
D23	ADD7	LUT Address	
D22	ADD6	LUT Address	
D21	ADD5	LUT Address	
D20	ADD4	LUT Address	
D19	ADD3	LUT Address	
D18	ADD2	LUT Address	
D17	ADD1	LUT Address	
D16	ADD0	LUT Address (LSB)	See Table5.
D15	Dummy	Dummy Data "0"	
D14	Dummy	Dummy Data "0"	
D13	Dummy	Dummy Data "0"	
D12	Dummy	Dummy Data "0"	
D11	Dummy	Dummy Data "0"	
D10	Dummy	Dummy Data "0"	
D9	DATA9	LUT Data (MSB)	
D8	DATA8	LUT Data	
D7	DATA7	LUT Data	
D6	DATA6	LUT Data	
D5	DATA5	LUT Data	
D4	DATA4	LUT Data	
D3	DATA3	LUT Data	
D2	DATA2	LUT Data	
D1	DATA1	LUT Data	
D0	DATA0	LUT Data (LSB)	

Table2: Command table (CMD5 to CMD0: 6-bit)

DATA name	Parameter	Remarks
CMD5	Selection of WRITE/READ mode "1": WRITE mode "0": READ mode	In case of "0", must be set as follows. CMD4: "1", CMD3: "0", CMD2: "1" CMD1: "0", CMD0: "0"
CMD4	Must be set to "1".	-
CMD3	Selection of Random/Sequential Address WRITE "1": Random Address WRITE "0": Sequential Address WRITE	-
CMD2	Must be set to "1".	-
CMD1	Selection of Individual/Simultaneous RGB setting "1": Individual RGB setting "0": Simultaneous RGB setting	"1": Select the color by using ADD9 and ADD8. (See Table4.) "0": ADD9 and ADD8 are invalid.
CMD0	Must be set to "0".	-

Table3: Command Combination table (CMD5 to CMD0: 6-bit)

CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	Mode
1	1	1	1	1	0	Random Address WRITE, Individual RGB setting
1	1	1	1	0	0	Random Address WRITE, Simultaneous RGB setting
1	1	0	1	1	0	Sequential Address WRITE, Individual RGB setting
1	1	0	1	0	0	Sequential Address WRITE, Simultaneous RGB setting
0	1	0	1	0	0	READ mode

*Another combinations are prohibited, and may cause function error.

Table4: Address table (ADD9 to ADD0: 10-bit)

DATA name	Parameter	Remarks
ADD9	Color Selection ADD[9:8]= 0:0 Red 0:1 Green 1:0 Blue 1:1 ON/OFF selection of Gamma Correction	In case of "ADD[9:8]=1:1", ON/OFF of Gamma correction can select according to the GMA[2:0]. (See Table6 and Table7.)
ADD8		
ADD7		
ADD6		
ADD5	LUT Address 256 address = 00h - FFh	If ADD[9:8] = 1:1, ADD[7:0] must be set to 00h.
ADD4		
ADD3		
ADD2		
ADD1		
ADD0		

Table5: Data table (DATA15 to DATA0: 16-bit)

DATA	DATA name	Parameter	Remarks
DATA15	Dummy	Dummy Data Must be set to "0".	-
DATA14	Dummy		
DATA13	Dummy		
DATA12	Dummy		
DATA11	Dummy		
DATA10	Dummy		
DATA9	DATA9	[MSB] 10-bit LUT Data 000h - 3FFh [LSB]	-
DATA8	DATA8		
DATA7	DATA7		
DATA6	DATA6		
DATA5	DATA5		
DATA4	DATA4		
DATA3	DATA3		
DATA2	DATA2		
DATA1	DATA1		
DATA0	DATA0		

Table6: Gamma correction table (DATA15 to DATA0: 16bit)

DATA	DATA name	Parameter	Remarks
DATA15	Dummy	Dummy Data Must be set to "0".	-
DATA14	Dummy		
DATA13	Dummy		
DATA12	Dummy		
DATA11	Dummy		
DATA10	Dummy		
DATA9	Dummy		
DATA8	Dummy		
DATA7	Dummy		
DATA6	Dummy		
DATA5	Dummy		
DATA4	Dummy		
DATA3	Dummy		
DATA2	GMA2	[MSB] GMA Data [LSB]	See Table7.
DATA1	GMA1		
DATA0	GMA0		

Table7: Control code GMA[2:0]

GMA2	GMA1	GMA0	Function
0	0	0	No correction
0	0	1	Correction according to the LUT Data.

*Another combinations are prohibited, and may cause function error.

Note1: When writing and reading the LUT data, a noise may appear on the display image. In order to prevent the noise appearing on the display, following measures should be performed.

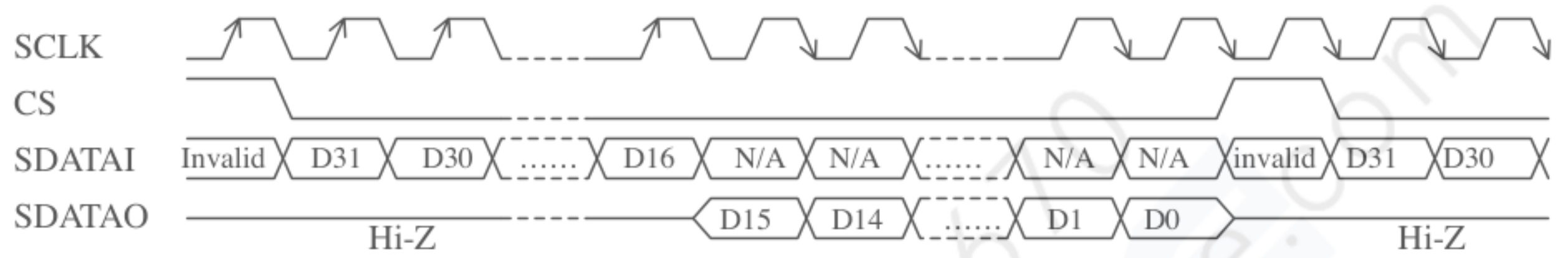
- (1) The LUT data should be rewritten during invalid period of pixel data (See "4.8 INPUT SIGNAL TIMINGS").
- (2) The LUT data should be rewritten while the LUT data is invalid.

Note2: Because the LUT data isn't stored in the LCD module, transfer the data every power-on.

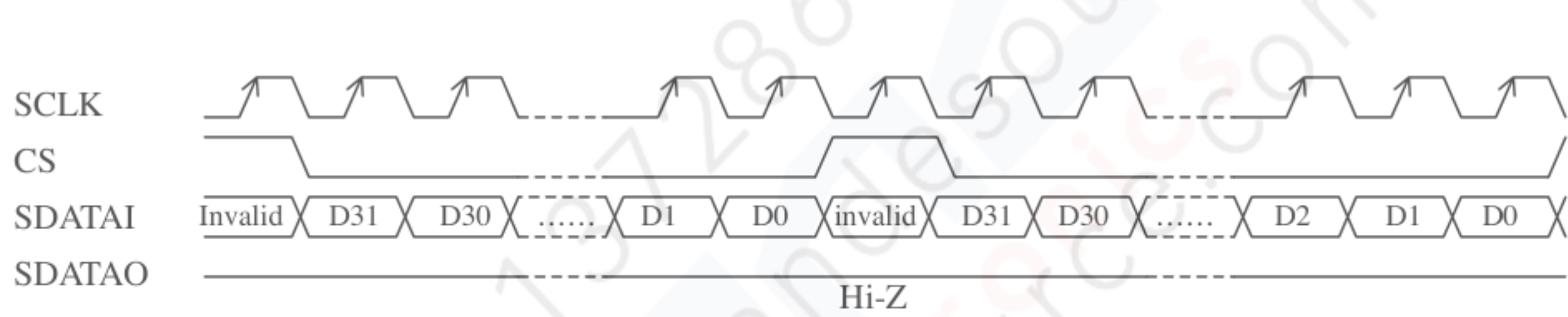
4.11 LUT SERIAL COMMUCATION TIMINGS

4.11.1 Timing Chart

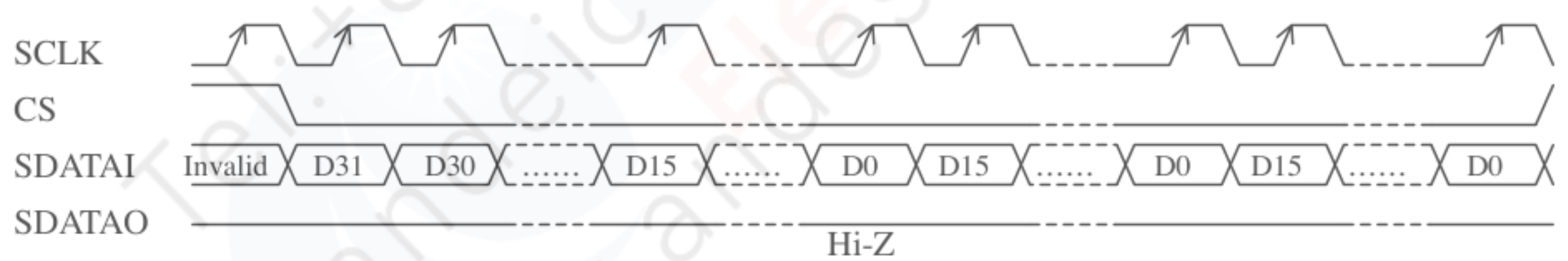
(1) READ Timing Chart



(2) Random Address WRITE Timing Chart



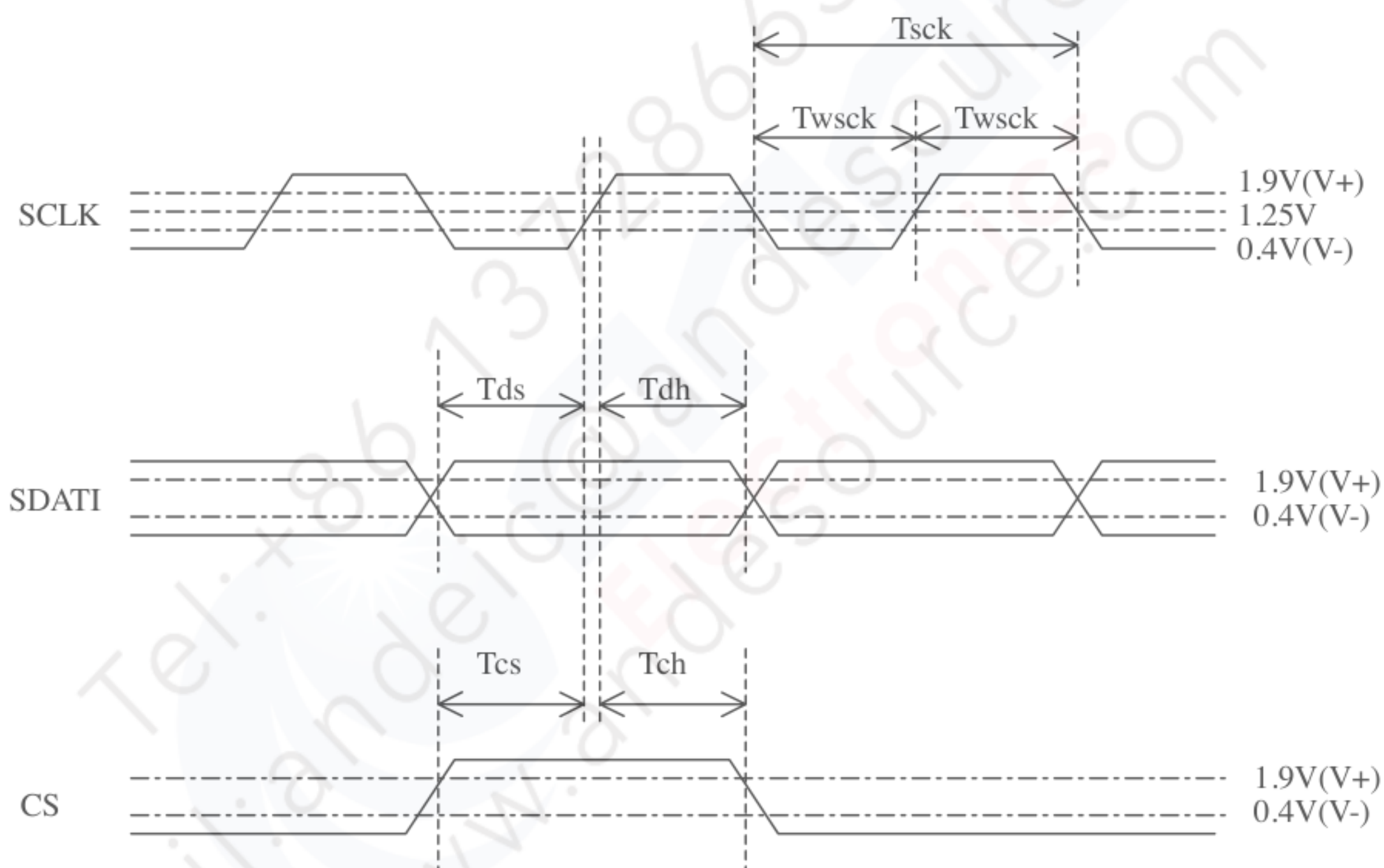
(3) Sequential Address WRITE Timing Chart



4.11.2 Timing specifications

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
SCLK Frequency	1/Tsck	-	-	5	MHz	-
SCLK Pulse Width (WRITE)	Twscck	50	-	-	ns	-
SCLK Pulse Width (READ)	Twscck	5	-	-	tc	Note1
SDATI-SCLK Setup Time	Tds	50	-	-	ns	-
SDATI-SCLK Hold Time	Tdh	50	-	-	ns	-
CS-SCLK Setup Time	Tcs	50	-	-	ns	-
CS-SCLK Hold Time	Tch	50	-	-	ns	-

Note1: At the READ of the serial communication mode, the SCLK Pulse Width (Twscck) must be greater than 5CLK (5 tc's). (See "4.8.1 Timing characteristics".)



Note2: During the serial communication mode, the display noise may appear because of rewriting the data. To avoid this, rewrite the data in the blanking timing. The external noise may cause the data change, refresh the data regularly according to need.

4.12 OPTICS



4.12.1 Optical characteristics

(Note1, Note2)

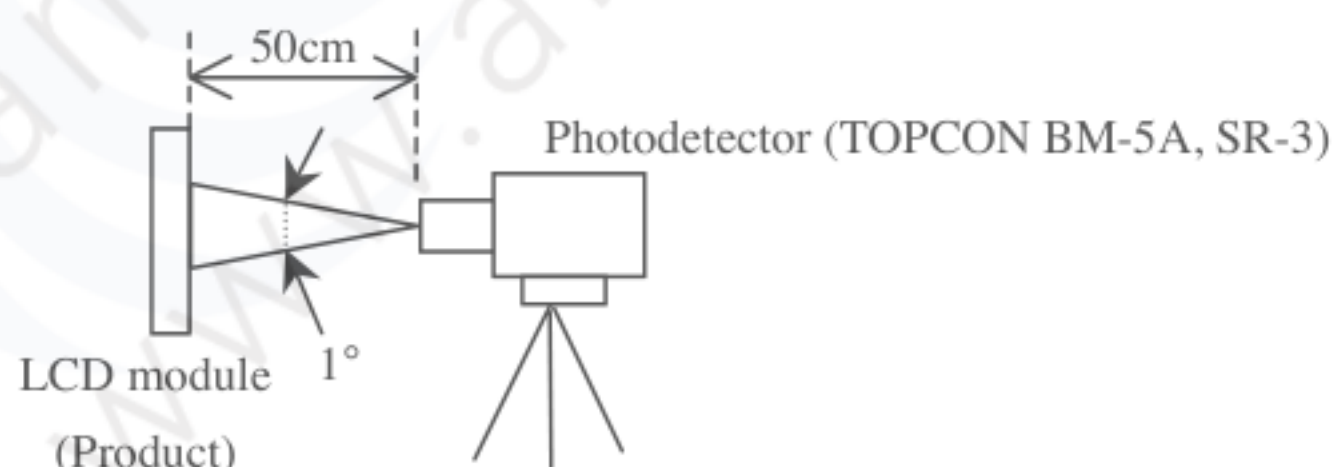
Parameter	Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks
Luminance	White at center $\theta_R = 0^\circ, \theta_L = 0^\circ, \theta_U = 0^\circ, \theta_D = 0^\circ$	L	200	250	-	cd/m ²	SR-3	-
Contrast ratio	White/Black at center $\theta_R = 0^\circ, \theta_L = 0^\circ, \theta_U = 0^\circ, \theta_D = 0^\circ$	CR	300	450	-	-	SR-3	Note3
Luminance uniformity	-	LU	-	-	1.3	-	BM-5A	Note4
Chromaticity	White	x coordinate	Wx	0.313	-	-	SR-3	Note5
		y coordinate	Wy	0.329	-	-		
	Red	x coordinate	Rx	0.65	-	-		
		y coordinate	Ry	0.33	-	-		
	Green	x coordinate	Gx	0.29	-	-		
		y coordinate	Gy	0.61	-	-		
	Blue	x coordinate	Bx	0.14	-	-		
		y coordinate	By	0.079	-	-		
Color gamut	$\theta_R = 0^\circ, \theta_L = 0^\circ, \theta_U = 0^\circ, \theta_D = 0^\circ$ at center, against NTSC color space	C	65	72	-	%		
Response time	Black to White	Ton	-	9	20	ms	BM-5A	Note6
	White to Black	Toff	-	11	20	ms		Note7
Viewing angle	Right	$\theta_U = 0^\circ, \theta_D = 0^\circ, CR \geq 10$	θ_R	70	85	-	BM-5A	Note8
	Left	$\theta_U = 0^\circ, \theta_D = 0^\circ, CR \geq 10$	θ_L	70	85	-		
	Up	$\theta_R = 0^\circ, \theta_L = 0^\circ, CR \geq 10$	θ_U	70	85	-		
	Down	$\theta_R = 0^\circ, \theta_L = 0^\circ, CR \geq 10$	θ_D	70	85	-		

Note1: These are initial characteristics.

Note2: Measurement conditions are as follows.

Ta = 25°C, VDD = 12.0V, IBL = 6.0mA/rms/lamp, Display mode: UXGA,
Horizontal cycle = 75.19kHz, Vertical cycle = 60.0Hz

Optical characteristics are measured after 20 minutes from working the product, in the dark room. Also measurement method for luminance is as follows.



Note3: See "4.12.2 Definition of contrast ratio".

Note4: See "4.12.3 Definition of luminance uniformity".

Note5: These coordinates are found on CIE 1931 chromaticity diagram.

Note6: Product surface temperature: TopF = 30°C

Note7: See "4.12.4 Definition of response times".

Note8: See "4.12.5 Definition of viewing angles".

4.12.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

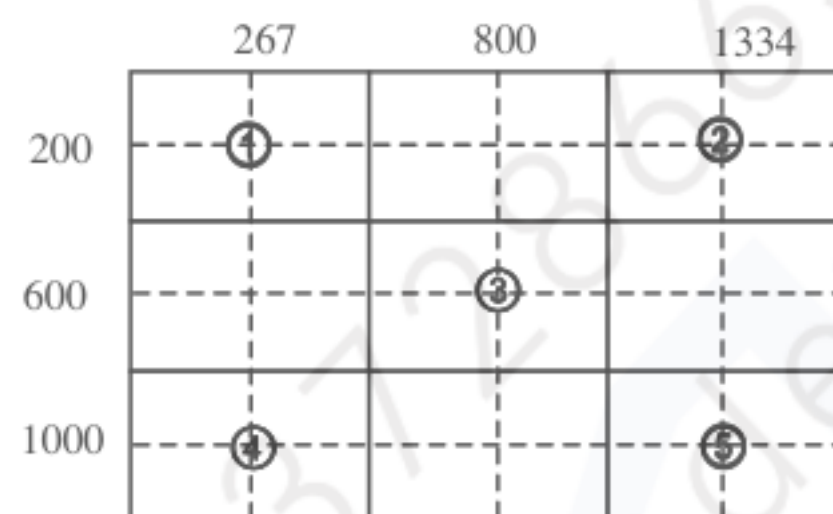
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.12.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

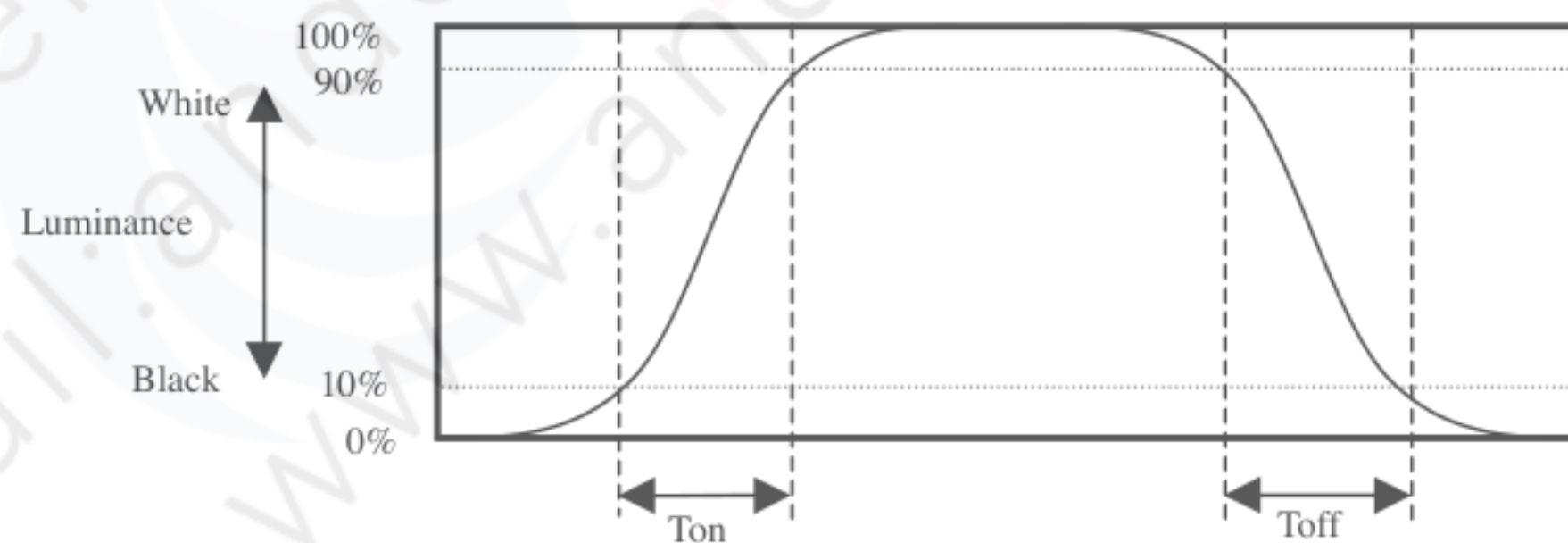
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

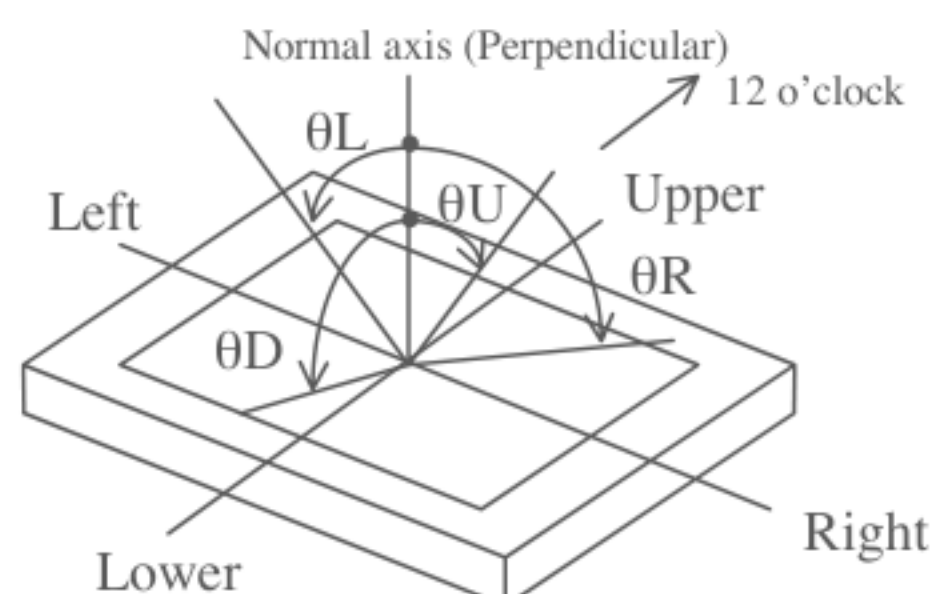


4.12.4 Definition of response times

Response time is measured, the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).



4.12.5 Definition of viewing angles

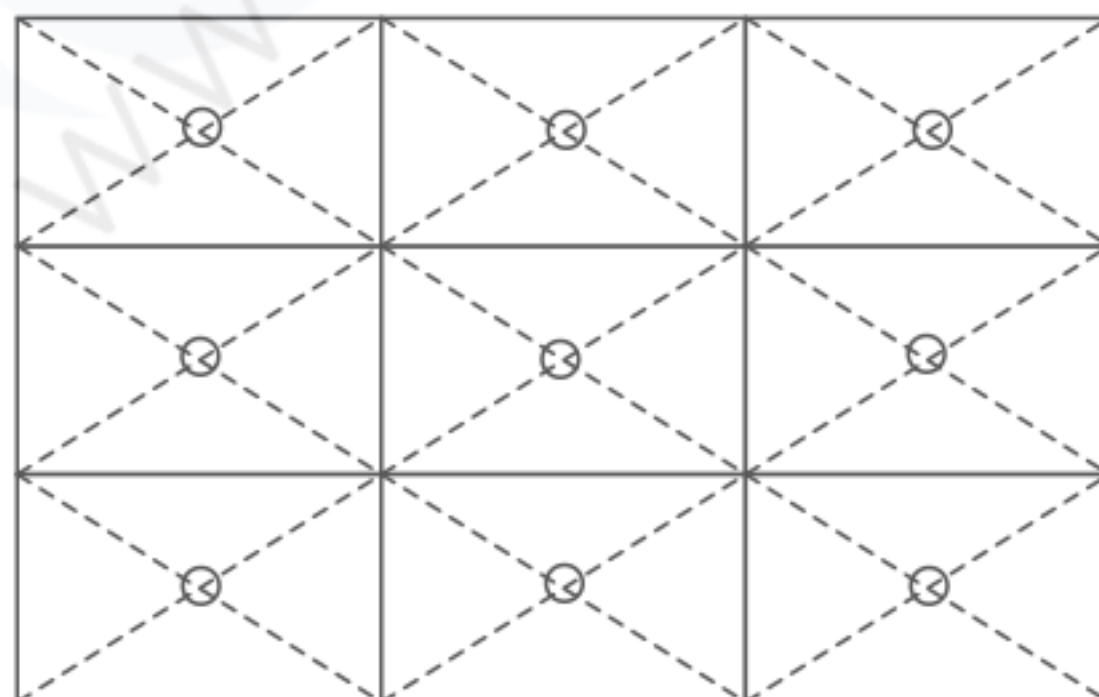


5. RELIABILITY TESTS

Test item		Condition	Judgment	Note1
High temperature and humidity (Operation)		① $60 \pm 2^{\circ}\text{C}$, RH = 60%, 240hours ② Display data is white.	No display malfunctions	
Heat cycle (Operation)		① $0 \pm 3^{\circ}\text{C}$...1hour $55 \pm 3^{\circ}\text{C}$...1hour ② 50cycles, 4hours/cycle ③ Display data is white.		
Thermal shock (Non operation)		① $-20 \pm 3^{\circ}\text{C}$...30minutes $60 \pm 3^{\circ}\text{C}$...30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.		
Vibration (Non operation)		① 5 to 100Hz, 11.76m/s^2 ② 1 minute/cycle ③ X, Y, Z direction ④ 10 times each directions	No display malfunctions No physical damages	
Mechanical shock (Non operation)		① 294m/s^2 , 11ms ② X, Y, Z direction ③ 3 times each directions		
ESD (Operation)		① 150pF, 150Ω , $\pm 10\text{kV}$ ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	No display malfunctions	
Dust (Operation)		① Sample dust: No.15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval		
Low pressure	Non-operation	① 15 kPa (Equivalent to altitude 13,600m) ② $-20^{\circ}\text{C} \pm 3^{\circ}\text{C}$...24 hours ③ $+60^{\circ}\text{C} \pm 3^{\circ}\text{C}$...24 hours	No display malfunctions	
	Operation	① 53.3 kPa (Equivalent to altitude 4,850m) ② $0^{\circ}\text{C} \pm 3^{\circ}\text{C}$...24 hours ③ $+55^{\circ}\text{C} \pm 3^{\circ}\text{C}$...24 hours		

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.

Note2: See the following figure for discharge points



6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS" and "6.3 ATTENTIONS", after understanding this contents!**



This sign has the meaning that customer will be injured by himself or the product will sustain a damage, if customer has wrong operations.



This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.



This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS



*** Do not touch the working backlight. Customer will be in danger of an electric shock.**



*** Do not touch the working backlight. Customer will be in danger of burn injury.**
*** Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: To be not greater 294m/s² and to be not greater 11ms, Pressure: To be not greater 19.6N)**

6.3 ATTENTIONS



6.3.1 Handling of the product

- ① Take hold of both ends without touch the circuit board when customer pulls out products (LCD modules) from inner packing box. If customer touches it, products may be broken down or out of adjustment, because of stress to mounting parts.
- ② Do not hook cables nor pull connection cables such as lamp cable and so on, for fear of damage.
- ③ If customer puts down the product temporarily, the product puts on flat subsoil as a display side turns down.
- ④ Take the measures of electrostatic discharge such as earth band, ionic shower and so on, when customer deals with the product, because products may be damaged by electrostatic.
- ⑤ The torque for mounting screws must never exceed 0.735 N·m. Higher torque values might result in distortion of the bezel. And the length of mounting screws from surface of plate must be ≤ 5.3mm.
- ⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area) except mounting hole portion.
Bends or twist described above and undue stress to any portion except mounting hole portion may cause display un-uniformity.
- ⑦ Do not press or rub on the sensitive display surface. If customer clean on the panel surface, NEC recommends using the cloth with ethanolic liquid such as screen cleaner for LCD.

- ⑧ Do not push-pull the interface connectors while the product is working, because wrong power sequence may break down the product.

6.3.2 Environment

- ① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in antistatic pouch in room temperature, because of avoidance for dusts and sunlight, if customer stores the product.
- ② In order to prevent dew condensation occurring by temperature difference, the product packing box must be opened after leave under the environment of an unpacking room temperature enough. Because a situation of dew condensation occurring is changed by the environmental temperature and humidity, evaluate the leaving time sufficiently. (Recommendation leaving time: 6 hour or more with packing state)
- ③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
- ④ This product is not designed as radiation hardened.
- ⑤ Use an original protection sheet on the product surface (polarizer). Adhesive type protection sheet should be avoided, because it may change color or properties of the polarizer.

6.3.3 Characteristics

The following items are neither defects nor failures.

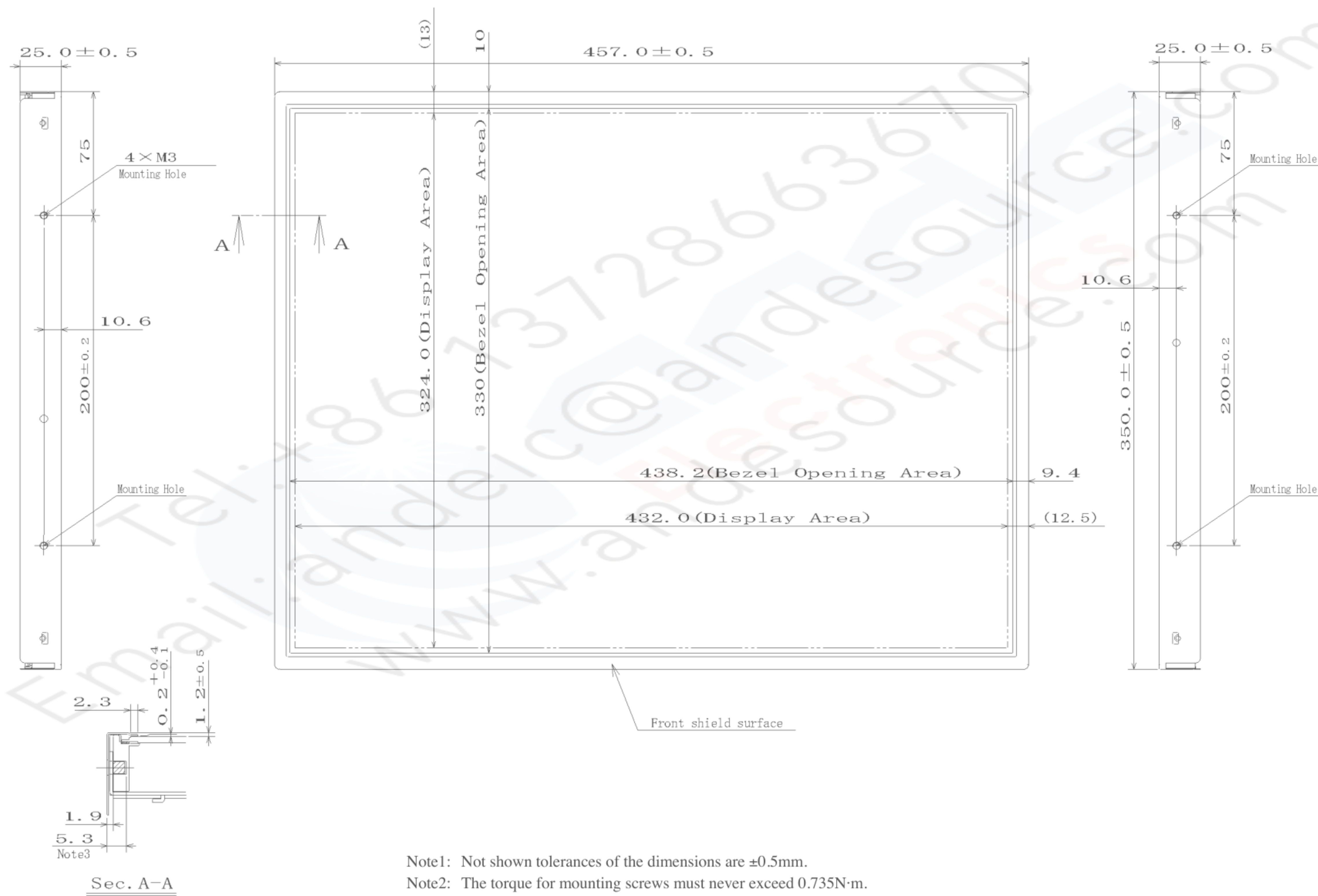
- ① Response time, luminance and color may be changed by ambient temperature.
- ② The LCD may be seemed luminance non-uniformity, flicker, vertical seam or small spot by display patterns.
- ③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
- ④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
- ⑤ The display color may be changed by viewing angle because of the use of condenser sheet in the backlight.
- ⑥ Optical characteristics may be changed by input signal timings.
- ⑦ The interference noise of input signal frequency for this product's signal processing board and luminance control frequency of customer's backlight inverter may appear on a display. Set up luminance control frequency of backlight inverter so that the interference noise does not appear.

6.3.4 Other

- ① All GND, backlight inverter ground (GNDB), VDD and backlight inverter power supply voltage (VDDb) terminals should be used without a non-connected line.
- ② Do not disassemble a product or adjust volume without permission of NEC.
- ③ Pay attention not to insert waste materials inside of products, if customer uses screwnails.
- ④ Pack the product with original shipping package, because of avoidance of some damages during transportation, when customer returns it to NEC for repair and so on.
- ⑤ The LCD module by itself or integrated into end product should be packed and transported with display in the vertically position. Otherwise the display characteristics may be impaired.

7. OUTLINE DRAWINGS

7.1 FRONT VIEW



Note1: Not shown tolerances of the dimensions are ± 0.5 mm.

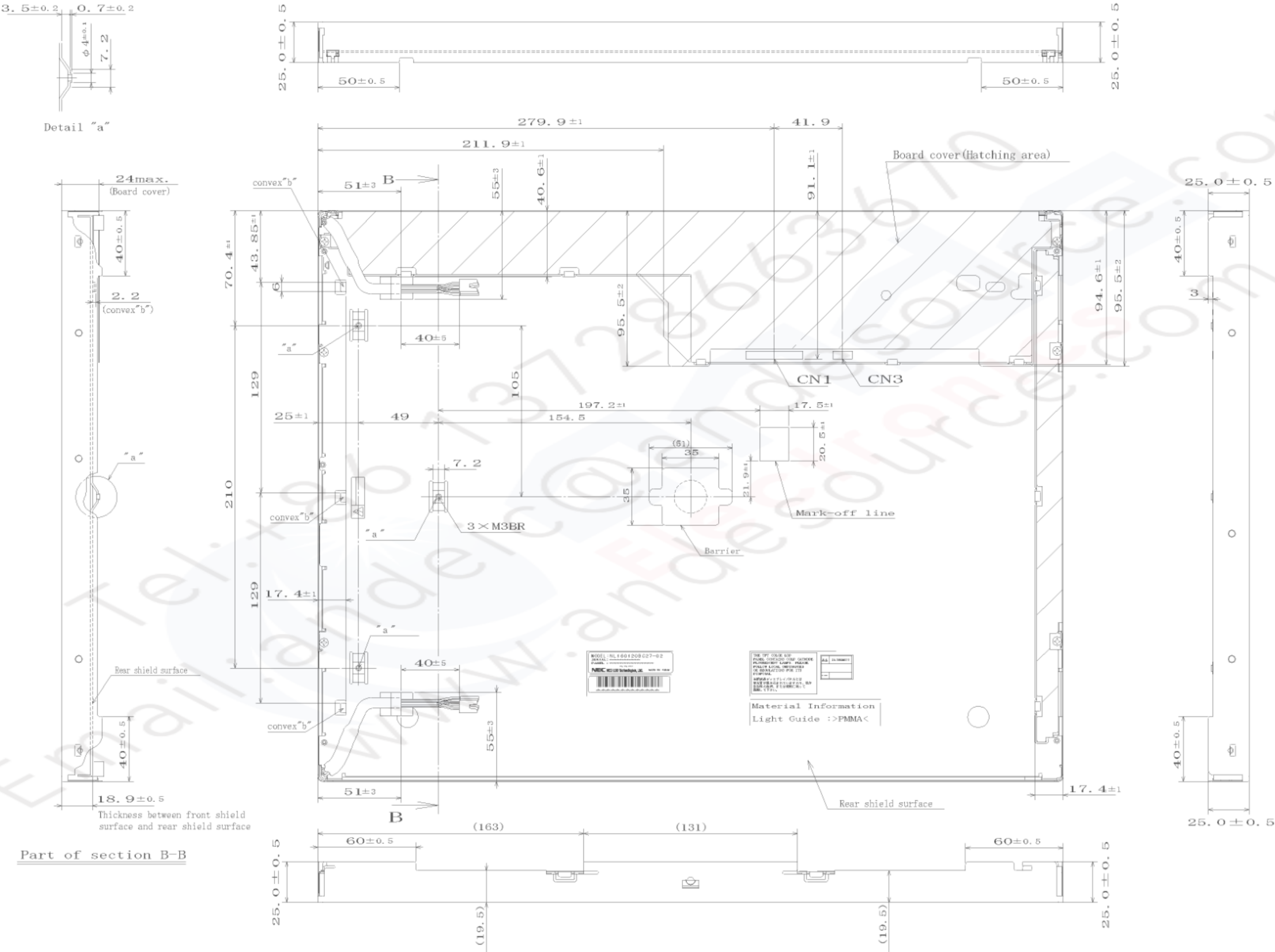
Note2: The torque for mounting screws must never exceed 0.735 N·m.

Note3: The length of mounting screws from surface of plate must be ≤ 5.3 mm.

Note4: The values in parentheses are for reference.

Unit: mm

7.2 REAR VIEW



- Note1: Not shown tolerances of the dimensions are $\pm 0.5\text{mm}$.
Note2: The torque for mounting screws must never exceed $0.735\text{N}\cdot\text{m}$.
Note3: The values in parentheses are for reference.

Unit: mm